STIC Search Report
EIC 2800

STIC Database Tracking Number: 101919

TO: Monica Lewis **Location: CP3 3B07** **Art Unit : 2822** **Friday, August 22, 2003** **Case Serial Number: 09/863737**	**From: Irina Speckhard** **Location: EIC 2800** **CP4-9C18** **Phone: 308-6559** **irina.speckhard@uspto.gov**

Search Notes

Examiner Lewis,

Please find attached first-pass prior-art search results from the patent and non-patent abstract databases. The results were based on claims and statements of technical problems and solutions. Tagged records might be worth your review as well as the rest of the references provided.

If you need further searching or have questions or comments, please let me know.

Thank you,

Irina Speckhard

6426 101919

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 8/20/03 Serial # 09/863,737 Priority Application Date 3/4/98

Your Name M. Lewis Examiner # _____

AU 2822 Phone 305-3743 Room Plaza 3-3807

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case? 08-21-03 A09:49 IN

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___ _____

Teaching Refs ___ _____

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-8

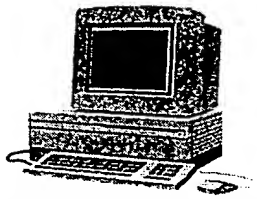
Problem: See Page 1 lines 14-30
" " 2 " 1-30
" " 3 " 1-16

Solution: " " 4 " 20-30
" " 4 " 1-29

Staff Use Only		Type of Search		Vendors	
Searcher:	Jack Lavelle	Structure (#)		STN	✓
Searcher Phone:		Bibliographic	✓	Dialog	✓
Searcher Location:	STIC-EIC2800, CP4-9C18	Litigation		Questel/Orbit	
Date Searcher Picked Up:	8/22/03	Fulltext		Lexis-Nexis	
Date Completed:	8/22/03	Patent Family		WWW/Internet	
Searcher Prep/Rev Time:	125	Other		Other	
Online Time:	118				

EIC2800

Search Results Feedback Form (Optional)



Scientific & Technical Information Center

The search results generated for your recent request are attached. If you have any questions or comments (compliments or complaints) about the scope or the results of the search, please contact ***the EIC searcher*** who conducted the search ***or contact***:

Jeff Harrison, Team Leader, 306-5429

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example:* 2830

- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art **not found**:*
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Search results were not useful in determining patentability or understanding the invention.

Other Comments:

Drop off completed forms in **CP4-9C18,** or send to **Jeff Harrison, CP4-9C18.**

```
     (FILE 'HOME' ENTERED AT 14:02:15 ON 22 AUG 2003)

     FILE 'REGISTRY' ENTERED AT 14:02:28 ON 22 AUG 2003
L1           19 SEA ABB=ON  PLU=ON  F.O.SI/MF OR F O SI/MF
L2           50 SEA ABB=ON  PLU=ON  AL/MF
L3         2864 SEA ABB=ON  PLU=ON  N.TI/MF OR N TI/ELF

     FILE 'CAPLUS' ENTERED AT 14:03:35 ON 22 AUG 2003
L4          539 SEA ABB=ON  PLU=ON  L1 OR SIOF OR ((SI OR SILICON)(W)(OXYFLUORI
                DE OR OXIDE FLUORIDE))
L5           24 SEA ABB=ON  PLU=ON  L4 AND (WIRING OR WIRE)(3A)(LAYER#### OR
                FILM#### OR COAT##### OR MULTILAYER##### OR MULTI(W)LAYER#####
                OR SPACER#### OR INTERLAYER OR INTER(W)LAYER#####)
L6            1 SEA ABB=ON  PLU=ON  L5 AND (WIRING OR WIRE)(3A)(GAP OR
                OPENING)
                D BIB AB
L7           23 SEA ABB=ON  PLU=ON  L5 NOT L6
L8            0 SEA ABB=ON  PLU=ON  L7 AND (JUXTAPOSE OR UNIT###### OR
                CONNECT)(3A)(WIRING OR WIRE)
L9            5 SEA ABB=ON  PLU=ON  L7 AND (L2 OR L3)
L10           5 DUP REM L9 (0 DUPLICATES REMOVED)
                D BIB AB TOT
L11          18 SEA ABB=ON  PLU=ON  L7 NOT L9
L12           0 SEA ABB=ON  PLU=ON  L11 AND (LAYER##### OR FILM##### OR
                COAT###### OR MULTILAYER###### OR MULTI(W)LAYER###### OR
                SPACER##### OR INTERLAYER OR INTER(W)LAYER##### OR MULTIPLE(W)L
                AYER)(3A)METALLIZAT##########
L13           0 SEA ABB=ON  PLU=ON  L11 AND (FIRST OR ONE OR TWO OR SECOND)(3A)
                (INSULAT######### OR DIELECTR#######)
L14          18 DUP REM L11 (0 DUPLICATES REMOVED)
                D BIB AB TOT
```

L6 ANSWER 1 OF 1 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:34440 CAPLUS
DN 132:72331
TI Production method of semiconductor device.
IN Koyanagi, Kenichi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000012539	A2	20000114	JP 1998-169778	19980617
	JP 3104750	B2	20001030		
PRAI	JP 1998-169778		19980617		

AB The title method involves forming a **SiOF** insulator film on a substrate, forming **openings** for a **wiring** in the **SiOF film**, removing the F in the **SiOF** film via the surface of the openings, treating the surface of the openings with an O plasma, and forming a metal for the **wiring** in the **openings**. Specifically, F removal may be carried out by treating with a H plasma. A strong bonding between the metal and insulator film is obtained.

L10 ANSWER 1 OF 5 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:335418 CAPLUS
DN 138:330180
TI Formulation and use of an etchant for manufacturing **wires** of a thin **film** transistor array substrate
IN Park, Hong-Sick; Kang, Sung-Chul
PA Samsung Electronics Co., Ltd., S. Korea
SO PCT Int. Appl., 65 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2003036377	A1	20030501	WO 2002-KR112	20020124

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG

PRAI KR 2001-65326 A 20011023
AB First, a lower film of AlNd Alloy and an upper film of MoW alloy are deposited in succession and then patterned by an etchant including 0.1-10% HNO3, 55-65% H3PO4, 5-20% AcOH, 0.1-5% stabilizer, and the balance ultra-pure water, to form a gate wire including a gate line, a gate electrode and a gate pad on a substrate. Next, a gate insulating film, a semiconductor layer and an ohmic contact layer are formed in succession, and then, MoW alloy is deposited and patterned by an etchant including 0.1-10% HNO3, 55-65% H3PO4, 5-20% AcOH, 0.1-5% stabilizer, and the balance ultra-pure H2O, to form a data wire including a data line intersecting the gate line, a source electrode, a drain electrode, and a data pad. Next, a passivation layer is deposited and patterned to form contact holes for exposing the drain electrode, the gate pad, and the data pad, resp. Then, IZO is deposited and patterned to form a pixel electrode, an auxiliary gate pad and an auxiliary data pad elec. connected to the drain electrode, the gate pad, and the data pad, resp.
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L10 ANSWER 2 OF 5 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:452300 CAPLUS
DN 139:29347
TI Semiconductor damascene process improving interconnection reliability of contact holes
IN Ajisawa, Haruhiko
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2003168733	A2	20030613	JP 2001-365289	20011129
PRAI	JP 2001-365289		20011129		

AB The process comprises these steps; forming contact holes in interlayer insulation films by etching, eliminating etching-stopper **layers** to expose **wiring layers** on the hole bottom, eliminating etching deposits from the wiring surface, etching as-formed overhang parts at tapered edges of stopper layers, depositing barrier metals in the bottom and sidewalls of the holes, and filling plug metals in the holes.

L10 ANSWER 3 OF 5 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:840832 CAPLUS
DN 135:351582
TI Semiconductor integrated circuit and its fabrication
IN Saito, Tatsuyuki; Ohashi, Naoshi; Imai, Toshinori; Noguchi, Junji; Tamaru, Takeshi
PA Hitachi Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 42 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001319928	A2	20011116	JP 2000-135041	20000508
	TW 483105	B	20020401	TW 2001-90105990	20010314
	US 2001045651	A1	20011129	US 2001-850162	20010508
PRAI	JP 2000-135041	A	20000508		

AB A method for fabricating a semiconductor integrated circuit having a wiring resistant to migration involves prepg. a semiconductor substrate having a Si oxide film and a Si nitride **film**, forming a **wiring** recess in the oxide and nitride films, depositing a Cu film on the oxide film via a barrier layer, selectively removing the barrier layer and Cu **film** to form a **wiring**, and selectively forming a W cap **film** on the **wiring**. An integrated circuit fabricated by the above method is also described.

L10 ANSWER 4 OF 5 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:29163 CAPLUS
DN 134:94320
TI Fabrication of semiconductor device with low dielectric constant layer.
IN Yamagishi, Nobuhisa
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001007203	A2	20010112	JP 1999-175355	19990622
PRAI	JP 1999-175355		19990622		

AB The process includes forming an insulator **layer** for covering 1st **wiring** on a semiconductor (e.g., Si) substrate, forming contact holes on the insulator **layer** and reaching 1st **wiring**, forming a plug material layer on the insulator layer, processing the plug

material layer to form plugs protruded from the insulator layer and contacting with contact holes resp., and forming an interlayer insulator layer at the circumference side of the plugs for embedding the latter; the interlayer insulator layer is an org. low-dielec.-const. layer.

L10 ANSWER 5 OF 5 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:166321 CAPLUS
DN 132:201861
TI Semiconductor device with electromigration resistance and their manufacture
IN Iguchi, Manabu
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000077413	A2	20000314	JP 1998-248451	19980902
PRAI	JP 1998-248451		19980902		

AB The barrier metal layers in the title semiconductor devices, comprising buried metal (e.g. Cu) **wirings**, consist of **multilayered** metals. The barrier metal **layer** contacting the **wiring** show strong adhesion with the wiring and that contacting the interlayer insulator layer is a diffusion prevention layer. The devices are manufd. by formation of a 1st and a 2nd insulator layers on a substrate, formation of a groove in the 2nd insulator layer utilizing the 1st insulator layer as an etch stopper, formation of a Cu diffusion prevention layer as the 1st barrier metal layer, formation of a metal layer showing strong adhesion with Cu as the 2nd barrier metal layer, and deposition of Cu until filling the groove, followed by chem. mech. polishing of the Cu and the 1st and the 2nd barrier metal layers down to the surface of the 2nd insulator layer. Another insulator layer having low dielec. const. may also be formed in between the 2 insulating layers. Cu wirings with excellent electromigration resistance are formed.

L14 ANSWER 1 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2003:118324 CAPLUS
DN 138:162145
TI Semiconductor integrated circuit device
IN Tamaru, Tsuyoshi; Oomori, Kazutoshi; Miura, Noriko; Aoki, Hideo; Oshima, Takayuki
PA Japan
SO U.S. Pat. Appl. Publ., 29 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003030146	A1	20030213	US 2002-214579	20020809
	JP 2003060030	A2	20030228	JP 2001-244152	20010810
PRAI	JP 2001-244152	A	20010810		

AB A semiconductor integrated circuit device comprises a semiconductor substrate, an interlayer insulating film including **SiOF** films formed on a main surface of the semiconductor substrate, a wiring groove formed by dry etching of the interlayer insulating **film**, and a Cu **wiring** buried in the wiring groove by a damascene method wherein a silicon oxynitride film is provided between a silicon nitride film serving as an etching stopper layer for the dry etching and the **SiOF** film so that free F generated in the **SiOF** film is trapped with the silicon oxynitride film.

L14 ANSWER 2 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:66759 CAPLUS
DN 136:127550
TI Deposition of a silicon containing insulating thin **film** to cover **wiring** interconnections
IN Oku, Taizo; Aoki, Junichi; Yamamoto, Youichi; Koromokawa, Takashi; Maeda, Kazuo
PA Canon Sales Co., Inc., Japan; Semiconductor Process Laboratory Co., Ltd.
SO Eur. Pat. Appl., 33 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1174915	A2	20020123	EP 2001-116694	20010717
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 2002028584	A1	20020307	US 2001-903764	20010713
	JP 2002164346	A2	20020607	JP 2001-220232	20010719
	US 2002127869	A1	20020912	US 2002-126666	20020422
PRAI	JP 2000-221379	A	20000721		
	JP 2000-281263	A	20000918		
	JP 2000-221380	A	20000721		
	US 2001-904868	A3	20010716		

AB The present invention relates to a film forming method of forming an interlayer insulating film having a low dielec. const. to cover a wiring. In construction, an insulating **film** for covering a **wiring** is formed on the substrate by plasma treating a film forming gas, that consists of any one selected from a group consisting of

alkoxy compd. having Si-H bonds and siloxane having Si-H bonds and any one O-contg. gas selected from a group consisting of O2, N2O, NO2, CO, CO2, and H2O, to react.

L14 ANSWER 3 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:781446 CAPLUS
DN 135:337846
TI Design and fabrication of a semiconductor device comprising via holes and grooves formed by etching an organic low dielectric constant film
IN Nambu, Hidetaka
PA Japan
SO U.S. Pat. Appl. Publ., 16 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001034137	A1	20011025	US 2001-836286	20010418
	JP 2001308175	A2	20011102	JP 2000-120337	20000421
	TW 486755	B	20020511	TW 2001-90109694	20010420
PRAI	JP 2000-120337	A	20000421		

AB A method is presented for manufg. a semiconductor device having a **multi-layer wiring** structure including a photo-resist pattern having a prescribed opening dimension which is formed on an interlayer insulating film composed of an org. low dielec. const. film and a Si-contg. insulating film durable to an NH3-based gas in which the Si-contg. insulating film is dry etched using the photo-resist pattern as a mask and then the org. low dielec. const. film is etched by dry etching with NH3 or an NH3-contg. gas using the Si-contg. insulating film as an etching mask to form an opening part having a high aspect ratio and a substantially vertical cross-section shape. The described method prevents bowing of the cross-section shape of a via hole formed in an org. low dielec. const. film as well preventing a shoulder drop effect in a Si-contg. insulating film used as an etching mask for the org. low dielec. const. film and provides a method for fabricating the semiconductor device which is capable of etching the org. low dielec. const. film with a high amt. of precision.

L14 ANSWER 4 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:710227 CAPLUS
DN 135:265579
TI Fabrication of semiconductor device
IN Hiramatsu, Katsunori
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 16 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001267294	A2	20010928	JP 2000-72116	20000315
PRAI	JP 2000-72116		20000315		

AB The title method involves forming a contact hole reaching a doped layer in a Si oxide film and plasma processing using a gas contg. hydrogen (such as steam) to convert a fluorocarbon polymer side-wall protective film to a hydrocarbon polymer side-wall protective film. The method is useful for

suppressing the formation of under cuts of an underlayer **wiring layer** at the bottom of a contact hole in ashing with an O plasma during the formation of a contact hole in a Si oxide film by plasma etching using a pattern of a photoresist film and a fluorocarbon gas.

L14 ANSWER 5 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:723632 CAPLUS
DN 133:289918
TI Semiconductor device having fluorine diffusion prevention layer and its manufacture
IN Matsuura, Masasumi; Goto, Kinya
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000286262	A2	20001013	JP 1999-87521	19990330
	US 2001021557	A1	20010913	US 2001-785248	20010220
	US 6551921	B2	20030422		
PRAI	JP 1999-87521	A	19990330		
	US 1999-359654	A3	19990726		

AB An insulating **film** between an upper **wire** and a lower wire in the device comprises a lower F-contg. SiO2 (**SiOF**) layer, an intermediate layer, and an upper layer. The static capacitance of the insulating film is smaller in comparison with the case where a F-free SiO2 layer is used. The intermediate layer contains Si-N bonds or Si-H bonds or N atoms (e.g., a SiON layer) and prevents the diffusion of the F atoms in the **SiOF** layer. If the F atoms diffuse and reach the upper wire comprising Ti/TiN buffer layers and an Al alloy layer, a TiF compd. is generated and the upper wire comes off from the insulating film. The intermediate layer also prevents moisture from going into the **SiOF** layer while the upper layer is planed by CMP (chem. mech. polishing) using water.

L14 ANSWER 6 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1999:814114 CAPLUS
DN 132:43819
TI Electronic device having barrier metal layer and its manufacture method
IN Muroyama, Masakazu
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11354464	A2	19991224	JP 1998-157899	19980605
PRAI	JP 1998-157899		19980605		

AB The device is equipped with a F-contg. SiO2 layer successively coated with a barrier metal layer contg. Ta, Zr, TaN, and/or ZrN and a metal layer. The manuf. method involves (1) forming the SiO2 layer on a substrate and (2) successively forming the barrier metal layer and the metal layer thereon. The device shows improved adhesion between the SiO2 layer and the barrier metal layer and peeling prevention of the metal layer. The

device may be useful for an interlayer insulating **film** or an inner **wiring** in a semiconductor device, etc.

L14 ANSWER 7 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1999:325610 CAPLUS
DN 130:345924
TI Formation of wiring of semiconductor device.
IN Yamada, Yoshiaki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 11135503	A2	19990521	JP 1997-294634	19971027
PRAI JP 1997-294634		19971027		

AB The title method involves forming a Wiring of an Al-based metal layer, heat treating to grow the grains of the metal layer, and forming a **SiOF** film. Optionally, a F-frequency insulator film such as silica may be formed prior to the heat treatment. Specifically, the **SiOF** film may be formed using a silane gas (or TEOS), F-type gas such as CF4, C2F6, NF3, or SiF4 (or TEFS), and O2. The F diffusion into the **wiring layer** is prevented.

L14 ANSWER 8 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1998:816388 CAPLUS
DN 130:89276
TI Fabrication of semiconductor device containing interlayer insulating film having a low dielectric constant
IN Miyajima, Shuji; Ui, Akio
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 10340897	A2	19981222	JP 1997-149154	19970606
PRAI JP 1997-149154		19970606		

AB The title process comprises: (1) prepg. a semiconductor substrate with a Ti-contg. metal wiring formed on its main surface; (2) forming a 1st oxidn. film contg. F on the main surface by using a 1st gas having a weak etching ability with respect to Ti; (3) decreasing the amt. of impurities remaining in the 1st oxidn. film, e.g., by discharge in an O-contg. gas; and (4) forming a 2nd oxidn. film contg. F on the 1st oxidn. film by using a 2nd gas having an etching ability with respect to Ti stronger than that of the 1st gas. The 2nd oxidn. film is prepd. by high-d. plasma CVD. Etching damage of the wiring during the formation of the 2nd insulating film is prevented, and the dielec. const. of the insulating film can be decreased.

L14 ANSWER 9 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1998:735333 CAPLUS
DN 130:31796
TI Multilayer interconnection structure and its formation method.

IN Yokoyama, Takashi; Yamada, Yoshiaki; Kishimoto, Koji
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10303298	A2	19981113	JP 1997-109291	19970425
	JP 3109449	B2	20001113		
	CN 1198015	A	19981104	CN 1998-101625	19980422
	US 2001003060	A1	20010607	US 1998-66115	19980423
	US 6287956	B2	20010911		
PRAI	JP 1997-109291	A	19970425		

AB A planar multilayer interconnection structure comprises a no. of **wiring layers** on a semiconductor substrate, an oxide film contg. F for filling between the **wiring layers**, and an oxide planar film free of F on the oxide film contg. F. Addnl., a SOG film may be formed on the oxide planar film. A method for forming the above structure involves forming a 1st **wiring layer** on a semiconductor substrate via an insulator film, forming a **SiOF** film, forming a middle insulator film of an oxide film free of F, forming a SOG film to planarize the middle insulator film, dry etching back the SOG and middle insulator films using a F-contg. gas such as CF4, C2F6, NF3, or SiF4, forming a contact hole to reach the 1st **wiring layer**, and forming a 2nd **wiring layer** contacting the 1st **wiring layer**.

L14 ANSWER 10 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1998:227123 CAPLUS
DN 128:303002
TI Semiconductor device having **wiring** buried in insulator **film** and its fabrication method
IN Muroyama, Masakazu
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10098102	A2	19980414	JP 1996-252541	19960925
PRAI	JP 1996-252541		19960925		

AB The title device comprises a 1st insulator film of a fluorinated silicon oxide **film** having a buried **wiring** and a 2nd insulator film of a fluorinated silicon oxide film having a F content less than that for the 1st insulator film or from a film free of F. A method for fabricating the device involves CVD of the 1st and 2nd insulator films. The insulator films has a high bonding strength.

L14 ANSWER 11 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1997:772566 CAPLUS
DN 128:56387
TI Formation method of insulator film.
IN Muroyama, Masakazu
PA Sony Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09312333	A2	19971202	JP 1996-126618	19960522
PRAI JP 1996-126618		19960522		

AB A method for forming an insulator **film** to bury a **wiring** on a substrate involves plasma CVD of a Si oxide underlay film optionally contg. a low concn. of F and then a Si fluoride oxide overlay film. Specifically, the underlay and overlay films may be formed using gases having Si-H and Si-F bonds, resp. A film having a low water permeability is formed.

L14 ANSWER 12 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1997:385276 CAPLUS
DN 127:43473
TI Bilayered interlayer insulating film with high moisture resistance
IN Tsutsumi, Yoichi
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09116005	A2	19970502	JP 1995-269715	19951018
PRAI JP 1995-269715		19951018		

AB The insulating **film**, formed on a **wiring**, comprises a Si fluoroxide film and an amorphous Si oxide film coating. The insulating film inhibits generation of fluoric acid which causes a corrosion of the wiring.

L14 ANSWER 13 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1997:324220 CAPLUS
DN 127:27861
TI **Multilayer wiring** board and its manufacture
IN Furusawa, Kenji; Kusukawa, Kikuo; Honma, Yoshio
PA Hitachi, Ltd., Japan; Hitachi Chemical Co., Ltd.
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09082799	A2	19970328	JP 1995-235000	19950913
PRAI JP 1995-235000		19950913		

AB The wiring board has several metal (alloy) wiring patterns whose sides are successively laminated with a F-contg. Si compd. elec. insulating layer and an org. Si compd. elec. insulating layer to bury the spaces between the patterns. The manuf. of the above wiring board involving chem. mech. polishing with a Ce oxide particle-contg. polisher is also claimed. Flat wiring boards with low elec. capacitance between neighboring wirings are obtained by the method at low cost.

L14 ANSWER 14 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1997:124002 CAPLUS
DN 126:138061
TI Manufacture of fluorine-containing silicon oxide electric insulating film by plasma vapor deposition
IN Tamura, Yoshihiro
PA Anelva Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08330293	A2	19961213	JP 1995-156974	19950530
PRAI JP 1995-156974		19950530		

AB The title method comprises (1) introducing gaseous O to a deposition chamber where a substrate is placed or to a plasma generating chamber which is spaciously continuous to the deposition chamber to form O plasma, (2) introducing a F-contg. Si compd. gas (X) and a H-contg. a Si compd. gas (Y) there to form a F-contg. Si oxide elec. insulating thin film on the substrate by plasma vapor deposition while the flow of X to (X + Y) is controlled to 1-50%. In the above method, the elec. insulating film may be formed only from X in the presence of previously formed O and H plasma from gaseous O and H while the flow of H to X is controlled to 200-400%. The app. for the above methods is also claimed. The method is useful for lamination of elec. insulating **films** on **wiring** patterns in elec. circuits without etching them.

L14 ANSWER 15 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1996:508791 CAPLUS
DN 125:156208
TI Semiconductor apparatus with interlayer insulating film structure
IN Hasegawa, Toshiaki
PA Sony Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08162528	A2	19960621	JP 1995-3727	19950113
PRAI JP 1994-238821		19941003		

AB The app. comprises an insulating substrate successively **coated** with a **wiring** and 1st insulating **film**, and 2nd insulating film with lower sp. inductive capacity on the wiring. The app. may comprises 3rd insulating **film** (under the **wiring**) made of Si (nitr)oxide, and/or Si nitride, and 4th insulating film (under the 3rd insulating film) made of F-contg. Si oxide, polysiloxane, poly(p-xylylene), fluorocarbons, and/or polyimide. The wiring has high reliability due to inhibited corrosion of the 2nd insulating film and poisoned via.

L14 ANSWER 16 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1996:302397 CAPLUS
DN 124:358415

TI Semiconductor integrated circuit
IN Ichikawa, Jinko; Tsuneno, Katsumi; Masuda, Hiroo; Sato, Hisako; Nakamura, Takahide; Kunitomo, Hisaaki
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08064677	A2	19960308	JP 1994-201226	19940826
PRAI JP 1994-201226		19940826		

AB The circuit consists of a semiconductor substrate having pitch wirings with width .gtoreq.0.8 .mu.m and thickness 0.3-1.0 .mu.m. The circuit showed high transistor d.

L14 ANSWER 17 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1996:215404 CAPLUS
DN 124:303531
TI Properties of fluorinated silicon oxide films formed using fluorotriethoxysilane for interlayer dielectrics in multilevel interconnections
AU Homma, Tetsuya
CS ULSI Device Development Lab., NEC Corp., Kanagawa, 229, Japan
SO Journal of the Electrochemical Society (1996), 143(3), 1084-7
CODEN: JESOAN; ISSN: 0013-4651
PB Electrochemical Society
DT Journal
LA English
AB Properties of a fluorinated silicon oxide (**SiOF**) film for interlayer dielecs. in multilevel interconnections of ultralarge-scale integrated circuits (ULSIs) are investigated. The **SiOF** films are formed by a room temp. CVD deposition technique using fluorotriethoxysilane [FSi(OC2H5)3, FTES] and pure water as gas sources. **SiOF** film property changes by annealing at 400 or 900.degree. are studied. Although the Si-O bond absorption peak position in the FTIR spectrum is not changed by 400.degree. annealing, the peak position for the 900.degree. annealed **SiOF** films shifts to low wave nos. The full width at half-max. of the Si-O bond absorption peak increases by 400.degree. annealing, and it further increases by 900.degree. annealing. The tendency of the Si-F bond peak absorption coeff. change is inverse to the change of full width at half max., indicating that fluorine influences the Si-O bond nature. Other properties such as the fluorine at. concn., refractive index, etching rate, shrinkage, residual stress, and leakage c.d. are changed by the annealing. These property changes are due to changes in the chem. bonding structure. No crack was obsd. for the **SiOF films** formed on aluminum **wiring** patterns after 400.degree. annealing.

L14 ANSWER 18 OF 18 CAPLUS COPYRIGHT 2003 ACS on STN
AN 1996:132178 CAPLUS
DN 124:189844
TI Characteristics of **SiOF** films formed using tetraethylorthosilicate and fluorotriethoxysilane at room temperature by chemical vapor deposition
AU Homma, Tetsuya
CS NEC Corporation, ULSI Device Development Laboratories, Kanagawa, 229,

Japan
SO Journal of the Electrochemical Society (1996), 143(2), 707-11
CODEN: JESOAN; ISSN: 0013-4651
PB Electrochemical Society
DT Journal
LA English
AB The characteristics of **SiOF** films deposited using tetraethylorthosilicate (TEOS) and fluorotriethoxysilane [FTES: FSi(OC2H5)3] at room temp. by CVD (RTCVD) were studied. The RTCVD technique uses FTES, TEOS, and pure H2O as gas sources. The **SiOF** films are deposited by changing the FTES concn. in TEOS and FTES gas mixts. The **SiOF** film deposition does not occur without the presence of FTES gas. The deposition rate increases with increasing the FTES concn., then sats. at .apprx.12 nm/min while the FTES concn. is 80%. The relation between the film deposition rate and the FTES percentage in TEOS and FTES gas mixt. is not linearly proportional. The deposited **SIOF** film properties such a refractive index, Si-O bond nature, residual OH content, etching rate (1:30 buffered HF), and leakage current are almost independent of the FTES concn. at 20-100%. Residual F concns. for the **SiOF** films deposited at the FTES concns. of 20, 50, 80, and 100% are 1.91 .times. 1021, 1.82 .times. 1021, 1.51 .times. 1021, and 1.51 .times. 1021 atom/cm3, resp. The conformability of the **SiOF** **films** on Al **wiring** patterns is .apprx.100%. The formation mechanism of **SiOF** film s then described in five chain reactions.

(FILE 'HOME' ENTERED AT 14:00:31 ON 22 AUG 2003)

FILE 'WPIX, INPADOC, JAPIO, PATOSEP, PATOSWO' ENTERED AT 14:00:44 ON 22 AUG 2003

E JP1998-091538/AP,PRN

L1 6 S E3-E4

L1 ANSWER 1 OF 6 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2000-008833 [01] WPIX
DNN N2000-008062 DNC C2000-001560
TI Wiring layer for semiconductor device - has layer insulation film with fluorine concentration higher in wiring portion than on wiring.
DC L03 U11
IN IMAI, K; ODA, N
PA (NIDE) NEC CORP; (NIDE) NIPPON ELECTRIC CO
CYC 4
PI JP 11289012 A 19991019 (200001)* 7p
CN 1231504 A 19991013 (200008)
KR 99082907 A 19991125 (200055)
US 6274476 B1 20010814 (200148)
US 2002011675 A1 20020131 (200210)
KR 320883 B 20020204 (200255)
ADT JP 11289012 A **JP 1998-91538 19980403**; CN 1231504 A CN 1999-103534 19990402; KR 99082907 A KR 1999-11693 19990402; US 6274476 B1 US 1999-275532 19990324; US 2002011675 A1 Div ex US 1999-275532 19990324, US 2001-863737 20010523; KR 320883 B KR 1999-11693 19990402
FDT US 2002011675 A1 Div ex US 6274476; KR 320883 B Previous Publ. KR 99082907
PRAI **JP 1998-91538 19980403**
AB JP 11289012 A UPAB: 20000112
NOVELTY - The fluorine concentration of SiOF layer insulation films (11,16) in the wiring portion are higher than fluorine concentration of SiOF layer insulation films (12,17) on wiring.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of semiconductor device.
USE - For semiconductor device with multilayered interconnection structure using SIOF as insulating film.
ADVANTAGE - Reduces wiring capacity. Prevents debonding of an interlayer film on the wiring.
DESCRIPTION OF DRAWING - The figure shows the sectional view of semiconductor device. (11,12,16,17) SiOF layer insulation films.
Dwg.1/14

L1 ANSWER 2 OF 6 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 167888007 INPADOC ED 20020218 EW 200207 UP 20020218 UW 200207
TI SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME
IN ODA NORIAKI; IMAI KIYOTAKA
INS ODA NORIAKI; IMAI KIYOTAKA
INA JP; JP
PA NEC CORPORATION
PAS NIPPON ELECTRIC CO
PAA JP
DT Patent
PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)
PI US 2002011675 AA 20020131
AI US 2001-863737 A 20010523
PRAI US 2001-863737 A 20010523
JP 1998-91538 A 19980403
US 1999-275532 A3 19990324
AB In a semiconductor device having a multilayer metallization structure using SiOF film as an interlayer insulating film, with respect to the interlayer insulating film, the fluorine concentration of SiOF films (11, 16) in a wiring gap portion in the same layer wiring is set to be higher

than the fluorine concentration of SiOF films (12, 17) between the upper and lower layer wirings (8, 15; 15, 20).

L1 ANSWER 3 OF 6 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 155729623 INPADOC ED 20010905 EW 200135 UP 20011015 UW 200141
TI SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME
IN ODA NORIAKI; IMAI KIYOTAKA
INS ODA NORIAKI; IMAI KIYOTAKA
INA JP; JP
PA NEC CORPORATION
PAS NIPPON ELECTRIC CO
PAA US
DT Patent
PIT USBA PATENT (NO PREVIOUS PRE-GRANT PUBLICATION)
PI US 6274476 BA 20010814
AI US 1999-275532 A 19990324
PRAI **JP 1998-91538 A 19980403**
AB In a semiconductor device having a multilayer metallization structure using SiOF film as an interlayer insulating film, with respect to the interlayer insulating film, the fluorine concentration of SiOF films (11, 16) in a wiring gap portion in the same layer wiring is set to be higher than the fluorine concentration of SiOF films (12, 17) between the upper and lower layer wirings (8, 15; 15, 20).

L1 ANSWER 4 OF 6 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1
AN 122089185 INPADOC ED 20000215 EW 200005 UP 20000215 UW 200005
TI SEMICONDUCTOR DEVICE AND MAKING PROCESS THEREOF
IN ODA NORIAKI; IMAI KIYOTAKA
INS NORIAKI ODA; KIYOTAKA IMAI
INA JP; JP
PA NEC CORP.
PAS NIPPON ELECTRIC CO
PAA JP
TL English
DT Patent
PIT CNA UNEXAMINED APPLIC. OPEN TO PUBLIC INSPECTION
PI CN 1231504 A 19991013
AI CN 1999-103534 A 19990402
PRAI **JP 1998-91538 A 19980403**

L1 ANSWER 5 OF 6 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 2
AN 119616821 INPADOC ED 20010327 EW 200112 UP 20010514 UW 200119
IN ODA NORIAKI; IMAI KYOTAKA
INS ODA NORIAKI; IMAI KYOTAKA
PA NIPPON DENKI KK
PAS NIPPON ELECTRIC CO
DT Patent
PIT JPB2 PUBLISHED REGISTERED PATENT SPECIFICATION
PI JP 3132557B B2 20010205
AI **JP 1998-91538 A 19980403**
PRAI **JP 1998-91538 A 19980403**

L1 ANSWER 6 OF 6 JAPIO (C) 2003 JPO on STN
AN 1999-289012 JAPIO
TI SEMICONDUCTOR DEVICE AND ITS MANUFACTURE
IN ODA NORIAKI; IMAI KIYOTAKA
PA NEC CORP
PI JP 11289012 A 19991019 Heisei
AI **JP 1998-91538** (JP10091538 Heisei) 19980403
PRAI **JP 1998-91538**19980403
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To obtain a semiconductor device in which a circuit operating speed does not become slow, whose power consumption is reduced and whose yield is enhanced by, a method wherein the fluorine concentration of an SiOF film in an interconnection interval part is made higher than the fluorine concentration of an SiOF film on an interconnection.
SOLUTION: A first-layer interconnection 8, a second-layer interconnection 15 and a third-layer interconnection 20 are formed sequentially from the lower part in such a way that they are composed of, e.g. barrier metal layers 5A, 5B, 5C composed of titanium in a film thickness of about 30 nm and titanium nitride in a film thickness of about 100 nm, aluminum films 6A, 6B, 6C in a film thickness of about 0.5 μm and titanium nitride films 7A, 7B, 7C in a film thickness of about 30 nm. In addition, low fluorine-concentration SiOF films 12, 17 have a fluorine concentration of less than 5 atomic %, and high fluorine-concentration SiOF films 11, 16 have a fluorine concentration of 5 atomic % or higher. In addition, plasma oxide films are formed between the low-fluorine-concentration SiOF film 12, the second-layer interconnection 15 as its upper-layer interconnection, the low-fluorine-concentration SiOF film 17 and the third-layer interconnection 20 as its upper-layer interconnection as to prevent corrosion from being generated due to the direct contact of the interconnections with fluorine.

```
 22aug03 12:32:28 User267149 Session D937.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2003/Aug W2
         (c) 2003 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2003/Aug W4
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
*File   6: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   8:Ei Compendex(R)  1970-2003/Aug W2
         (c) 2003 Elsevier Eng.  Info. Inc.
*File   8: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File  34:SciSearch(R) Cited Ref Sci  1990-2003/Aug W3
         (c) 2003 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2003/Jul
         (c) 2003 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2003/Aug W3
         (c) 2003 BLDSC all rts. reserv.
  File  94:JICST-EPlus  1985-2003/Aug W3
         (c)2003 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs  1983-2003/Jul
         (c) 2003 The HW Wilson Co.
  File 144:Pascal  1973-2003/Aug W2
         (c) 2003 INIST/CNRS
  File 305:Analytical Abstracts  1980-2003/Jul W4
         (c) 2003 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2003/Jul
         (c) 2003 DECHEMA
  File 350:Derwent WPIX  1963-2003/UD,UM &UP=200354
         (c) 2003  Thomson Derwent
  File 347:JAPIO  Oct 1976-2003/Apr(Updated 030804)
         (c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2003/Mar
         (c) 2003 European Patent Office
  File 371:French Patents  1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
```

Set	Items	Description
S1	20	AU=(NORIAKI, O? OR NORIAKI O?)
S2	11	AU=(KIYOTAKA, I? OR KIYOTAKA I?)
S3	0	S1 AND S2
S4	0	(S1 OR S2) AND (WIRING OR WIRE????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER?????)
S5	0	(S1 OR S2) AND (ALUMINIUM OR ALUMINUM OR AL)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)

```
  22aug03 13:33:35 User267149 Session D938.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2003/Aug W2
         (c) 2003 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2003/Aug W4
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
*File   6: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   8:Ei Compendex(R)  1970-2003/Aug W2
         (c) 2003 Elsevier Eng.  Info. Inc.
*File   8: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File  34:SciSearch(R) Cited Ref Sci  1990-2003/Aug W3
         (c) 2003 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2003/Jul
         (c) 2003 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2003/Aug W3
         (c) 2003 BLDSC all rts. reserv.
  File  94:JICST-EPlus  1985-2003/Aug W3
         (c)2003 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs  1983-2003/Jul
         (c) 2003 The HW Wilson Co.
  File 144:Pascal  1973-2003/Aug W2
         (c) 2003 INIST/CNRS
  File 305:Analytical Abstracts  1980-2003/Jul W4
         (c) 2003 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2003/Jul
         (c) 2003 DECHEMA
  File 350:Derwent WPIX  1963-2003/UD,UM &UP=200354
         (c) 2003  Thomson Derwent
  File 347:JAPIO  Oct 1976-2003/Apr(Updated 030804)
         (c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2003/Mar
         (c) 2003 European Patent Office
  File 371:French Patents  1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
```

Set	Items	Description
S1	104356	(WIRING OR WIRE????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER-???? OR INTER()LAYER?????)
S2	9430	(WIRING? ? OR WIRE????)(3N)(GAP? ? OR OPENING? ?)
S3	112509	S1:S2
S4	142359	(JUXTAPOSE?????? OR UNIT????? OR CONNECT??????)(3N)(WIRING? ? OR WIRE????)
S5	6122	(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI(-)LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER???-?? OR MULTIPLE()LAYER? ?)(3N)METALLIZAT???????
S6	184974	(ALUMINIUM OR ALUMINUM OR AL)(3N)(LAYER??? OR FILM??? OR C-OAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR -INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)
S7	30478	(TITANIUM OR TI)(3N)NITRIDE
S9	939	SIOF OR (SILICON OR SI)(3N)(OXYFLUORIDE OR OXIDE()FLUORIDE)
S10	470321	(INSULAT???????? OR DIELECTRIC????????)(3N)(LAYER??? OR FI-LM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPA-CER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LA-YER? ?)
S11	104992	(FIRST OR ONE OR TWO OR SECOND)(3N)(INSULAT???????? OR DIE-LECTR???????)
S12	2943	FLUORINE(3N)CONCENTRAT???????
S13	15455	S3 AND S4
S14	7	S13 AND S8
S15	7	RD (unique items)
S16	15448	S13 NOT S14
S17	1299	S16 AND S6
S18	49	S17 AND S7
S19	0	S18 AND S5
S20	0	S18 AND S9
S21	28	S18 AND S10
S22	9	S21 AND S11
S23	19	S21 NOT S22
S24	0	S23 AND S12
S25	19	RD S23 (unique items)
S26	58	S3 AND S9
S27	7	S26 AND S4
S28	7	RD (unique items)
S29	51	S26 NOT S27
S30	11	S29 AND S12
S31	10	S30 AND (S6 OR S7)
S32	3	RD (unique items)
S33	1	S30 NOT S31
S34	40	S29 NOT S30
S35	2	S34 AND S2
S36	2	RD (unique items)
S37	38	S34 NOT S35
S38	38	S37 AND S1
S39	31	S38 AND S10
S40	31	RD (unique items)
S41	0	S40 AND S12
S42	8	S40 AND S11
S43	8	RD (unique items)
S44	23	S40 NOT S42

15/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015380355
WPI Acc No: 2003-441296/200341
XRAM Acc No: C03-116777
XRPX Acc No: N03-352290
Etchant for, e.g. molybdenum, molybdenum alloy wire, comprises specified percentage of nitric acid, phosphoric acid, acetic acid, stabilizer and other ultra pure water
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KANG S; PARK H
Number of Countries: 100 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200336377	A1	20030501	WO 2002KR112	A	20020124	200341	B

Priority Applications (No Type Date): KR 200165326 A 20011023
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200336377	A1	E	65	G02F-001/136	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

Abstract (Basic): WO 200336377 A1
Abstract (Basic):
NOVELTY - An etchant for wire comprises nitric acid (0.1-10%); phosphoric acid (65-55%); acetic acid (5-20%); stabilizer (0.1-5%); and other ultra pure water.
DETAILED DESCRIPTION - An etchant for wire comprises nitric acid (0.1-10%); phosphoric acid (65-55%); acetic acid (5-20%); stabilizer (0.1-5%); and other ultra pure water. The stabilizer has a structure of formula M(OH)xLy.
M=zinc, tin, chromium, aluminum, barium, iron, titanium, silicon or boron;
L=water, NH3, CN, COR; NNR
R=1-5C alkyl;
x=2 or 3; and
y=0, 1, 2, 3.
INDEPENDENT CLAIMS are also included for:
(a) a method for manufacturing wire for display comprising depositing a first conductive film (2) of molybdenum or molybdenum alloy on a substrate; and etching the first conductive film using the etchant as above;
(b) a method of manufacturing a thin film transistor array panel comprising forming a gate wire including a gate line and a gate electrode; forming a gate insulating **layer** covering the gate **wire**; forming a semiconductor **layer** on the gate insulating layer of the gate electrode; and forming a data wire including a source electrode, a drain electrode and a data line on the semiconductor layer or the gate insulating layer; and

(c) a thin film transistor array panel, comprising a gate wire formed on an insulating substrate and including a gate line and a gate pad connected to the gate line; a gate insulating **layer** covering the gate **wire**; a semiconductor **layer** formed on the gate insulating **layer**; a data **wire** formed on the gate insulating layer or the semiconductor layer and including a data line, a source electrode connected to the data line and formed on the semiconductor layer, and a drain electrode formed on semiconductor layer disposed opposite the source electrode in relation to the gate electrode; a passivation **layer** covering the data **wire**; and a conductor pattern made of indium zinc oxide and formed in the passivation layer.

The gate wire or the data wire is formed with a first conductive film made of molybdenum or molybdenum alloy. The first conductive film is patterned using the etchant above.

USE - The etchant is used to etch molybdenum, molybdenum alloy, or molybdenum tungsten alloy, preferably molybdenum tungsten alloy (claimed).

ADVANTAGE - The inventive etchant etches wire of molybdenum or molybdenum alloy formed of a low resistant material and having low resistant contact feature with another material, to pattern the wire to provide a good taper structure and excellent evenness.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view showing an etched profile when molybdenum tungsten alloy film is etched using the etchant for wire above.

Film (2)

pp; 65 DwgNo 1/17

15/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014919157
WPI Acc No: 2002-739864/200280
XRAM Acc No: C02-209485
XRPX Acc No: N02-582866
Semiconductor device comprises wirings formed in **wiring** grooves, and **connector** formed integrally with **wirings** in via holes
Patent Assignee: HITACHI LTD (HITA)
Inventor: AOKI H; MIYAZAKI H; OHMORI K; OSHIMA T
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020100984	A1	20020801	US 2001987914	A	20011116	200280	B
KR 2002042458	A	20020605	KR 200174455	A	20011128	200280	
JP 2002164428	A	20020607	JP 2000362462	A	20001129	200280	

Priority Applications (No Type Date): JP 2000362462 A 20001129
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020100984	A1		35	H01L-021/4763	
KR 2002042458	A			H01L-021/3205	
JP 2002164428	A		24	H01L-021/768	

Abstract (Basic): US 20020100984 A1
Abstract (Basic):
NOVELTY - A semiconductor device comprises wirings formed in wiring grooves (20); and a connector formed integrally with the wirings in via holes for **connecting** the **wirings** and lower layer wirings.
The Young's modulus of the first dielectric layer in which the via holes are formed, is smaller than the Young's modulus of a second dielectric **layer** in which the **wiring** grooves are formed.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the production of the above semiconductor device comprising forming a first dielectric layer and a second dielectric layer; forming the via holes at predetermined regions of the first dielectric **layer** and forming the **wiring** grooves at predetermined regions of the second dielectric layer; and burying a conductive member inside the via holes and the wiring grooves.
USE - As a semiconductor device.
ADVANTAGE - The semiconductor device has a **multi-layered wiring** structure with a silicon oxide film that repulses strongly to the stress of copper.
DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of main portion of a semiconductor substrate showing the semiconductor device.
Wirings (14)
Via hole (16)
Stopper dielectric thin film (18)
Wiring grooves (20)
pp; 35 DwgNo 1/26

15/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014511164
WPI Acc No: 2002-331867/200237
Related WPI Acc No: 2002-331866; 2002-341991
XRAM Acc No: C02-095858
XRPX Acc No: N02-260589
Film forming method by preparing film forming gas consisting of alkoxy compound or siloxane and oxygen-containing gas, and forming silicon-containing insulating film on substrate by plasmanizing the film forming gas to react
Patent Assignee: CANON SALES CO INC (CANO); SEMICONDUCTOR PROCESS LAB CO LTD (SEMI-N); CANON HANBAI KK (CANO-N); HANDOTAI PROCESS KENKYUSHO KK (HAND-N)
Inventor: AOKI J; KOROMOKAWA T; MAEDA K; OKU T; YAMAMOTO Y
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1174915	A2	20020123	EP 2001116694	A	20010717	200237	B
JP 2002164346	A	20020607	JP 2001220232	A	20010719	200241	
KR 2002009440	A	20020201	KR 200143736	A	20010720	200254	
TW 503514	A	20020921	TW 2001117414	A	20010717	200337	

Priority Applications (No Type Date): JP 2000281263 A 20000918; JP 2000221379 A 20000721
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1174915	A2	E	33	H01L-021/316	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2002164346	A		18	H01L-021/316	
KR 2002009440	A			H01L-021/203	
TW 503514	A			H01L-021/765	

Abstract (Basic): EP 1174915 A2
Abstract (Basic):
NOVELTY - Film forming method involves:
(i) preparing a film forming gas consisting of alkoxy compound or siloxane having silicon-hydrogen bonds, and oxygen-containing gas including oxygen, nitrous oxide, nitrogen dioxide, carbon monoxide, carbon dioxide, or water; and
(ii) forming a silicon-containing insulating film on the substrate by plasmanizing the film forming gas to react.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:
(A) a semiconductor device manufacturing method which comprises preparing a substrate on a surface of which a wiring is formed, and forming a silicon-containing insulating **film** for covering the **wiring** by plasmanizing a **film** forming gas to react; and
(B) a semiconductor device in which a silicon-containing insulation film whose peak of an absorption intensity of an infrared rays is in a wave number 2270-2350/cm, whose film density is 2.25-2.4 g/cm3, and whose relative dielectric constant is 3.3-4.3, is formed on a substrate.
USE - For forming an insulating film for a semiconductor device.
ADVANTAGE - The method is capable of lowering a dielectric constant of an interlayer insulating film as a whole and suppressing a change of

the dielectric constant due to moisture absorption, while preventing corrosion of a wiring and an increase in a leakage current.

DESCRIPTION OF DRAWING(S) - The figure is a side view of a configuration of a plasma chemical vapor deposition film forming equipment employed in the inventive method.

Parallel-plate type electrodes (2, 3)

Substrate (20)

pp; 33 DwgNo 1/16

15/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014222216
WPI Acc No: 2002-042914/200206
XRPX Acc No: N02-031851
Semiconductor device interconnection structure comprising additional capacitors with capacitors formed at desired positions to make countermeasure for power source noise
Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA DENKI SANGYO KK (MATU)
Inventor: MORIWAKI T; SUZUKI R; TAMARU M
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1071130	A2	20010124	EP 2000115236	A	20000713	200206	B
JP 2001085630	A	20010330	JP 2000212973	A	20000713	200206	
KR 2001029950	A	20010416	KR 200040721	A	20000714	200206	
TW 483150	A	20020411	TW 2000114073	A	20000714	200313	

Priority Applications (No Type Date): JP 99200845 A 19990714
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1071130	A2	E	31	H01L-023/522	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				
JP 2001085630	A		20	H01L-027/04	
KR 2001029950	A			H01L-027/04	
TW 483150	A			H01L-027/08	

Abstract (Basic): EP 1071130 A2
Abstract (Basic):
NOVELTY - An insulating inter-layer film of silicon dioxide is formed between the through holes (B11,B12) in a silicon substrate and a metal inter-**wiring film** of **SiOF** is formed between metallic wiring (M11,M12). When the structure is used as a supplementary capacitor to power source wiring for a countermeasure against noise, one metallic **wiring** is **connected** to the power source potential and the other to another power source potential, while the structure is formed in the area where switching noise is generated.
DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is included for a method for manufacturing a semiconductor device.
USE - Forming a capacitor at a desired position to counter power source noises.
ADVANTAGE - Forming large capacity capacitors in a smaller area.
DESCRIPTION OF DRAWING(S) - The drawing shows a portion where a capacitor of a semiconductor device is formed according to a first embodiment
Through holes (B11,B12)
Metallic wiring (M11,M12)
pp; 31 DwgNo 1a/15

15/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06597371
WIRING STRUCTURE FOR SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME

PUB. NO.: 2000-183168 [JP 2000183168 A]
PUBLISHED: June 30, 2000 (20000630)
INVENTOR(s): YASUDA MAKOTO
APPLICANT(s): NEC CORP
APPL. NO.: 10-362468 [JP 98362468]
FILED: December 21, 1998 (19981221)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a multi-step wiring structure, capable of suppressing the generation and progress of EM phenomenon of Al.

SOLUTION: This wiring structure 40 is constituted by a lower wiring 44 formed on a base insulating film 42, an interlayer insulating film 46 formed on the wiring 44, a contact 48 which penetrates the **layer** 46, an upper **wiring** 50 **connected** with the **wiring** 44 via the contact 48. The layer 44 is constituted by an Al-Cu alloy **layer** which constitutes a **wiring** main body, a Ti layer 44b, and a TiN layer 44c. The layer 46 is constituted of a BPSG film 46a and an **SiOF** film 46b. The layer 50 is arranged between a contact and is constituted by a laminated barrier metal layer 52 having high (111) orientability, an Al-Cu alloy **layer** 50a constituting the **wiring** main body, a Ti layer 50b and a TiN layer 50c. The barrier metal layer 52 having high (111) orientability is constituted of a Ti layer 52a, having a film thickness of 20 nm and the TiN layer 52b the thickness of 40 nm for improving the (111) orientability and to suppress the generation and progress of EM phenomenon of Al.

15/3,AB/6 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06170298
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-111845 [JP 11111845 A]
PUBLISHED: April 23, 1999 (19990423)
INVENTOR(s): MATSUNOU TADASHI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 09-271134 [JP 97271134]
FILED: October 03, 1997 (19971003)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor device which can suppress impurity diffusion and infiltration of water or hydroxyl ions for improving its reliability.

SOLUTION: Formed on an element isolation insulating **film** 11 is a **wiring layer** 20 of a plurality of first metal wiring lines. Formed on the insulating film 11 and the first metallic **wiring layer** 20 are a silicon oxide film 31 added in high concentration of fluorine, a silicon nitride film 32 and an SiO2 film 33. The SiO2 film 33 higher in relative permittivity than the **SiOF** film 31 but lower than that of the silicon nitride film 32. Formed, in the **SiOF** film 31, silicon nitride film 32 and SiO2 film 33 is a via hole for **connection** with the first **wiring layer** 20. A W plug material 41 is embedded in the via hole. A second metal **wiring layer** 50 is formed on the SiO2 film 33.

15/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06020198
MULTILAYERED INTERCONNECTION STRUCTURE AND ITS FORMING METHOD

PUB. NO.: 10-303298 [JP 10303298 A]
PUBLISHED: November 13, 1998 (19981113)
INVENTOR(s): YOKOYAMA KOJI
YAMADA YOSHIAKI
KISHIMOTO KOJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-109291 [JP 97109291]
FILED: April 25, 1997 (19970425)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a multilayered interconnection structure which has an **SiOF** film as an interlayer insulating film, the excellent flatness and the high reliability by a method wherein an oxide film which does not contain fluorine and whose surface is levelled is formed on an oxide film which contains fluorine and fills the spaces between a plurality of **wiring layers** formed on a semiconductor substrate.

SOLUTION: 1st **wiring layers** 4 are formed on a semiconductor substrate with an insulating film therebetween. An **SiOF** film 6 containing fluorine and an intermediate insulating film 7 which does not contain fluorine are formed, and an SOG film 8 is formed and its surface is levelled. The surfaces of the SOG film 8 and the intermediate insulating film 7 are etched back by fluorine system gas, through-holes are formed at predetermined positions, and 2nd **wiring layers** electrically connected to the 1st **wiring layers** are formed. The intermediate insulating layer 7 improves the precision of the etching back using a levelled film such as the SOG film 8. Further, the penetration of moisture into the **SiOF** film 6 which has a high moisture absorption property is avoided. The increase of the dielectric constant of the **SiOF** film 6 can be avoided and the corrosion of a through-hole part wiring caused by moisture can be eliminated.

23/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015310210
WPI Acc No: 2003-371144/200335
XRAM Acc No: C03-098333
XRPX Acc No: N03-296019
Manufacture of semiconductor device having wiring, by forming conductive pattern through forming **wiring** grooves on **insulating film**, and forming barrier metal **layer** and **wiring** material **layer** on conductor pattern
Patent Assignee: SONY CORP (SONY); NAGASHIMA N (NAGA-I)
Inventor: NAGASHIMA N
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030022482	A1	20030130	US 2002157402	A	20020529	200335	B
KR 2002092203	A	20021211	KR 200230181	A	20020530	200335	
JP 2002359244	A	20021213	JP 2001164672	A	20010531	200335	

Priority Applications (No Type Date): JP 2001164672 A 20010531
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030022482	A1		6	H01L-021/44	
KR 2002092203	A			H01L-021/28	
JP 2002359244	A		5	H01L-021/3205	

Abstract (Basic): US 20030022482 A1
Abstract (Basic):
NOVELTY - A semiconductor device having wiring is manufactured by:
(i) forming a conductor pattern through forming wiring grooves on an **insulating film**; and
(ii) forming a barrier metal **layer** and a **wiring** material **layer** on the conductor pattern.
DETAILED DESCRIPTION - Manufacture of semiconductor device having wiring, comprises:
(a) forming a conductor pattern by forming wiring grooves (3a, 3b) on an **insulating film** (1, 2);
(b) forming a first barrier metal **layer** and a **wiring** material **layer** on the conductor pattern;
(c) forming a second barrier metal layer, so that a height of a surface of the barrier metal layer on protuberances of the conductor pattern is made equal or approximately equal to a height of the surface of the second barrier metal, on recesses of the conductor pattern;
(d) removing the second barrier metal layer on the protuberances of the conductor pattern;
(e) removing the **wiring** material **layer** on the protuberances of the conductor pattern; and
(f) removing the first barrier metal layer on the protuberances of the conductor pattern and the second barrier metal layer on the recesses of the conductor pattern.
USE - For manufacture of semiconductor device having wiring.
ADVANTAGE - The method provides semiconductor device, which forms **wiring** having uniform **film** thickness. It provides **wiring** of a wide line width as well as a pad, improving an increased convenience of designing circuitry, and avoiding problems

such as delay due to increase of wiring resistance.

DESCRIPTION OF DRAWING(S) - The figure is a schematic diagram illustrating a wiring groove forming process.

Insulating film (1, 2)

Wiring grooves (3a, 3b)

pp; 6 DwgNo 1A/2

23/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014212587
WPI Acc No: 2002-033284/200204
Related WPI Acc No: 1998-398068; 1999-009304; 2003-102345
XRAM Acc No: C02-009276
XRPX Acc No: N02-025543

Providing of void in spacing between wiring lines of semiconductor substrate, involves depositing conductive layers on the substrate, and subsequently configuring the conductive **layers** into adjacent **wiring** lines

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: GIVENS J H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6309946	B1	20011030	US 95550916	A	19951031	200204	B
			US 96723263	A	19960930		
			US 98207890	A	19981208		

Priority Applications (No Type Date): US 95550916 A 19951031; US 96723263 A 19960930; US 98207890 A 19981208
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6309946	B1		11	H01L-021/76	Div ex application US 95550916 Cont of application US 96723263 Cont of patent US 5835987

Abstract (Basic): US 6309946 B1
Abstract (Basic):

NOVELTY - A void between wiring lines of semiconductor substrate is provided by depositing conductive layers on the substrate; subsequently configuring the conductive **layers** to adjacent **wiring** lines; depositing a dielectric material on the substrate; and accumulating the dielectric material between edges of the extending tops of the wiring lines to seal off an elongated void area.

DETAILED DESCRIPTION - Providing void (32) in a spacing between wiring lines (34, 36, 74, 76) of semiconductor substrate involves depositing at least three conductive layers on the substrate comprising lower, middle, and an upper layer; subsequently configuring the conductive layers into at least two adjacent wiring lines, forming the lower and the middle layers to each have a lateral width less than a lateral width of the upper layer so that at least two adjacent elongated wiring lines each have a cross-sectional shape of a T, and laterally extending tops on the length of the two adjacent wiring lines; depositing dielectric material (86) on the substrate and the semiconductor at least two adjacent elongated wiring lines with the extending tops to form a **layer**; and causing the **dielectric** material to accumulate between edges of the laterally extending tops of the at least two wiring lines to seal off an elongated void area between the two elongated wiring lines.

USE - For providing void in spacing or for reducing the resistance capacitance (RC) delay between adjacent wiring lines of a semiconductor substrate.

ADVANTAGE - The method minimizes resistance-capacitance coupling. It provides void having low dielectric value of 1.0, or reduced line spacing, e.g. less than 1 or less than 0.5 microns. It provides line spacing that is as low as 0.1 microns. The controllably defined void(s) reduce the dielectric value in the spacing between adjacent wiring lines, thus reducing RC delay.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of the planarized substrate.

Void (32)

Wiring lines (34, 36, 74, 76)

Dielectric material (86)

pp; 11 DwgNo 13/13

23/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014211289
WPI Acc No: 2002-031986/200204
XRAM Acc No: C02-008929
Method for forming metal line
Patent Assignee: HYNIX SEMICONDUCTOR INC (HYNI-N)
Inventor: CHOI C J; KIM Y C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001063782	A	20010709	KR 9961870	A	19991224	200204	B

Priority Applications (No Type Date): KR 9961870 A 19991224
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001063782	A		1	H01L-021/28	

Abstract (Basic): KR 2001063782 A
Abstract (Basic):
NOVELTY - A method for forming a metal line is provided to improve the reliability wiring by forming a plug layer after forming a metal line layer.
DETAILED DESCRIPTION - An **interlayer dielectric**(32), a **wiring layer**(34), and a hard mask layer(35) are formed on a substrate(31). A contact hole for exposing the substrate(31) is formed by etching selectively the hard mask **layer**(35), the wiring **layer**(34), and the **interlayer dielectric**(32). A plug **layer** is formed within the contact hole. The substrate(31) is **connected** with the **wiring layer** by the plug **layer**. The **wiring layer**(34) is formed by laminating a **titanium/titanium nitride** layer(33) of 300 to 1000 angstrom and an **aluminium layer**(34) of 3000 to 10000 angstrom.
pp; 1 DwgNo 1/10

23/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012870806
WPI Acc No: 2000-042639/200004
XRAM Acc No: C00-011885
XRPX Acc No: N00-032289
Contact hole formation procedure in semiconductor device manufacture - involves embedding tungsten only in connection hole by chemical vapor deposition, after which **wiring layer** having **aluminum** alloy is formed
Patent Assignee: SEIKO EPSON CORP (SHIH)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11297822	A	19991029	JP 9897997	A	19980409	200004	B

Priority Applications (No Type Date): JP 9897997 A 19980409
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11297822	A		6	H01L-021/768	

Abstract (Basic): JP 11297822 A
NOVELTY - A **titanium nitride** layer (104) and is formed on **insulating film** (103) on silicon substrate. A connection hole (106) is formed on TiN **layer** (104) and **insulating film** (103). Then, tungsten (107) is embedded only in connection hole by chemical vapor deposition, after which **wiring layer** having **aluminum** alloy (108) is formed.
USE - In semiconductor device manufacture.
ADVANTAGE - As connection hole is formed after formation of **titanium nitride** layer, **titanium nitride** do not exist in the side wall of connection hole or via hole. Moreover when patterning aluminum alloy to produce eye gap is performed, a microgroove is not generated in the **connection** hole, hence **wiring** with high yield and reliability is obtained.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of semiconductor device manufacturing method. (103) **Insulating film**; (104) **Titanium nitride** layer; (106) Connection hole; (107) Tungsten; (108) Aluminum alloy.
Dwg.1/3

23/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011922473
WPI Acc No: 1998-339383/199830
XRPX Acc No: N98-265587
Semiconductor device manufacturing method - involves forming main **wiring layer** made of **aluminium** system material, on surface of thin base film embedding inside connection hole, by sputtering technique at high temperature
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10125778	A	19980515	JP 96275693	A	19961018	199830	B

Priority Applications (No Type Date): JP 96275693 A 19961018
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10125778	A		5	H01L-021/768	

Abstract (Basic): JP 10125778 A

The method involves forming a double layered barrier metal film (36) on the inner wall of a connection hole (33) formed in an **insulating film** (32) over a substrate (31), and as well as on the **insulating film**. A thin base film (10) is formed on the entire surface of the barrier metal film including in the connection hole, by sputtering process at a low temperature to prevent flow of film-forming substance.

The thin base **film** is made of **aluminium** system material or copper system material. The thin base film offers high wettability than a **titanium-nitride** layer (35) which is the surface layer of the barrier metal **film**. A main wiring **layer** (11) made of **aluminium** system material is formed on the surface of the thin base film, thereby embedding inside the connection hole, by sputtering technique at high temperature.

ADVANTAGE - Secures **connection** state of **wirings**. Improves reliability of semiconductor device.

Dwg.1/5

23/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011922392
WPI Acc No: 1998-339302/199830
XRPX Acc No: N98-265506
Semiconductor device with multilayered interconnection structure manufacturing method - involves interposing sublayer wiring containing **titanium** and **titanium nitride** between upper and lower **aluminium** alloy **layer**
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10125679	A	19980515	JP 96277783	A	19961021	199830	B

Priority Applications (No Type Date): JP 96277783 A 19961021
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10125679	A		9	H01L-021/3205	

Abstract (Basic): JP 10125679 A

The method involves forming an **insulating film** (12) on a semiconductor substrate (11). A sublayer wiring (14,15) containing **titanium** and **titanium nitride**, is interposed between upper and lower **aluminium** alloy **layer** (13,16).

The upper **aluminium** alloy **layer** is covered by an **interlayer insulating film** (18). A through-hole (19) is formed in the **interlayer insulating film**, in which a metal plug (21) is inserted, so that first and second **wiring layers** are electrically **connected** by the metal plug.

ADVANTAGE - Improves electromigration resistance. Prolongs substantial element life. Prevents disconnection and inferior connection.

Dwg.1/7

23/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011865399
WPI Acc No: 1998-282309/199825
XRAM Acc No: C98-087455
XRPX Acc No: N98-222843
Implanting wiring pattern formation method for semiconductor device e.g. LSIC - involves forming upper **aluminium** alloy **wiring layer** on **titanium nitride** film, such that its thickness is more than three times of width of **wiring** groove formed on **interlayer insulating film**
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10098039	A	19980414	JP 96271787	A	19960920	199825	B

Priority Applications (No Type Date): JP 96271787 A 19960920
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10098039	A		11	H01L-021/3205	

Abstract (Basic): JP 10098039 A

The method involves forming an **interlayer insulating film** (3) on surface of substrate. A connection hole (4), and a wiring groove (5) are formed in the **interlayer insulating film** at predetermined position. A **titanium nitride** film (6) is formed on the **interlayer insulating film**. An upper **Al**-alloy **wiring layer** (7) is formed on the entire surface of the substrate with thickness more than three times the width of the wiring groove. A bridge shape is formed on portion of **wiring** groove and **connection** hole. For formation of the bridge shape, a dummy pattern is formed near **connection** area of **wiring** groove and **connection** hole.

Then, high pressure reflow process is performed under inert gas environment thereby Al-alloy is filled up into the **wiring** groove and the **connection** hole. Then, the **interlayer insulating film** is subjected to chemo-mechanical polishing process. Thereby implanting wiring is formed inside the wiring groove.

ADVANTAGE - Facilitates formation of implanting wiring with high stability. Facilitates formation of bridge shape on portion of wiring groove with high stability.

Dwg.2/22

23/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011519344
WPI Acc No: 1997-495830/199746
XRAM Acc No: C97-157794
XRPX Acc No: N97-412994
Multilayered wiring structure formation for semiconductor device - involves using mixed gas to etch **interlayer insulating film** and **titanium nitride** film to form **connection** hole of **wiring** structure
Patent Assignee: NEC KYUSHU LTD (KYUN)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9232424	A	19970905	JP 9633888	A	19960221	199746	B

Priority Applications (No Type Date): JP 9633888 A 19960221
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9232424	A		5	H01L-021/768	

Abstract (Basic): JP 9232424 A

The method involves forming a wiring structure having a TiN film (3) as the upper most layer on a Si substrate (20). An **interlayer insulating film** (2) surmounts the upper surface of the substrate.

A connection hole is formed on **Al**-Si-Cu **film** (4) of the **wiring** structure, by etching the **interlayer insulating film** and the TiN film using the fluoro carbon group gas like CF4 and CHF3. To promote etching of TiN film, SF6, He and N2 are mixed to the fluorocarbon group gases.

ADVANTAGE - Improves reliability and speed electromigration. Prevents stress migration policy.

Dwg.1/3

23/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010777907
WPI Acc No: 1996-274860/199628
Related WPI Acc No: 2003-347366
XRAM Acc No: C96-087187
XRPX Acc No: N96-231246
Forming multilayer interconnection for semiconductor device - involves forming **aluminium@ wiring layer, titanium@ layer** as **nitride** barrier, **titanium nitride** anti-reflection **layer** and **interlayer insulating layer**
Patent Assignee: YAMAHA CORP (NIHG)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8115979	A	19960507	JP 94276046	A	19941014	199628	B

Priority Applications (No Type Date): JP 94276046 A 19941014
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8115979	A		5	H01L-021/768	

Abstract (Basic): JP 8115979 A

The method involves forming a lower part **wiring layer** (32a) which consists of an **aluminium** alloy **film** (14b), a **Ti** film for **nitride** prevention (14c) and a TiN film for a reflected prevention (14d). An **interlayer insulating film** (34) is formed hiding the lower part **wiring layer** by selection etching process using a resist layer as a mask.

The resist layer is then removed. The lower part **wiring layer** is **connected** to an upper part **wiring layer** through the **connection** hole. The base of the connection hole is then positioned in the TiN film.

ADVANTAGE - Reduces connection resistance of interlayer connection part. Reduces variation in connection resistance. Improves yield.

Dwg.4/9

23/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010528556
WPI Acc No: 1996-025509/199603
XRAM Acc No: C96-008451
XRPX Acc No: N96-021644
Mfr. of connection hole for highly integrated semiconductor device - comprises forming **aluminium wiring layer**, patterning by etching, and forming the connection hole in **insulating layer** deposited on **wiring layer**
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7297281	A	19951110	JP 94107692	A	19940422	199603	B

Priority Applications (No Type Date): JP 94107692 A 19940422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7297281	A		7	H01L-021/768	

Abstract (Basic): JP 7297281 A

The connection hole mfg. method is applicable to a substance (11), on which a **wiring** metal **layer** (12) of **Al** system is formed. Surface of **wiring layer** is exposed to the oxidising environment. An etching stop layer of TiN or **Ti** oxide **nitride** system is formed on the **wiring layer**. A non-reflecting film (14) is formed on the etching stop layer.

Patterning of the **wiring layer**, the etching stop layer and the reflected prevention layer is carried out to form the wiring structure (15). An **insulating film** (16) if formed on the **wiring layer**. A **connection** hole (19) is formed on the wiring structure.

ADVANTAGE - Obtains high etching selection ratio. Reduces time required for film formation. Improves reliability during wiring process. Improved yield. Reduces chip area and cost of mfr..

Dwg.1/4

23/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010233445
WPI Acc No: 1995-134702/199518
XRAM Acc No: C95-061998
XRPX Acc No: N95-106037

Multilayer interconnection structure of semiconductor devices e.g. LSI - uses second **wiring layer connected** to first **wiring layer** through **connection** hole with **titanium nitride** film at hole's bottom

Patent Assignee: YAMAHA CORP (NIHG)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7058110	A	19950303	JP 93219069	A	19930811	199518	B

Priority Applications (No Type Date): JP 93219069 A 19930811
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7058110	A		6	H01L-021/3205	

Abstract (Basic): JP 7058110 A

The structure is formed by an **insulating film** (14) hiding the surface of a semiconductor substrate (10). A connection hole (14A) is formed on the **insulating film**. A **wiring layer** (16) is formed to the **insulating film**, which is connected to the substrate. An **interlayer** insulating **film** (18) covers the **wiring layer** and the **insulating film**. The **wiring layer** is composed of a Ti **film** (16a), a TiON **film** (16b), an **Al film** (16c), a Ti film (16d) and a TiN film (16e). The setup is heat treated in a temperature ranging from 400-500 degree centigrade for 30 minutes. A connection hole (18A) is formed, with the TiN film as bottom (Z) of the second **connection** hole. A second **wiring layer** (20) is **connected** to the first **wiring layer**, through the second connection hole.

ADVANTAGE - Improves connection state of interlayer connection part; reduces junction leak current; and inhibits generation of aluminium hillocks and alloy pits.

Dwg.1/7

23/3,AB/12 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06262945
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 11-204526 [JP 11204526 A]
PUBLISHED: July 30, 1999 (19990730)
INVENTOR(s): SHINOMIYA HIDEO
SUGIMOTO SHIGEKI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 10-006240 [JP 986240]
FILED: January 16, 1998 (19980116)

ABSTRACT

PROBLEM TO BE SOLVED: To decrease the electrical resistance of a connecting hole by thinning the thickness of a film, which is deposited in the connecting hole by providing a metal **wiring**, the **connecting** hole which is formed to the upper surface of the metal wiring from the upper surface of a conducting film, a lubricating film, which facilitates the formation of the **wiring** in the **connecting** hole, and the like.

SOLUTION: Aluminum 34 which is used as a metal wiring is formed. A silicon dioxide film 35 is formed as the **interlayer insulating film** so as to embed the **aluminum** on the **insulating film**. A titanium **film** 36 is formed as a lubricating film on the upper surface of the silicon dioxide film 35. Furthermore, a **titanium nitride** film 37 is formed as the conducting film on the upper surface of the titanium film 36. Then, a connecting hole 38, which reaches the upper surface of the aluminum 34 from the upper surface of the **titanium nitride** film 37 is formed at a specified position. Aluminum 40, which becomes the second wiring, is formed on the entire surface on the **titanium nitride** 37. The **titanium nitride film** 37 prevents the **wire** breakdown of the aluminum 40 and improves the directivity of the aluminum 40. Furthermore, a titanium film 39 facilitates the in flow of the aluminum 40 into the connecting hole 38.

23/3,AB/13 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05971283
SEMICONDUCTOR DEVICE AND ORGANIC EL DISPLAY DEVICE

PUB. NO.: 10-254383 [JP 10254383 A]
PUBLISHED: September 25, 1998 (19980925)
INVENTOR(s): YAMAUCHI YUKIO
ARAI MICHIO
APPLICANT(s): TDK CORP [000306] (A Japanese Company or Corporation), JP (Japan)
SEMICONDUCTOR ENERGY LAB CO LTD [470730] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-053243 [JP 9753243]
FILED: March 07, 1997 (19970307)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor device, which is non-corroding and non- deteriorating, and allows a stable electric connection, reduces a specific resistance, and improves processability, by providing a barrier metal laminating **titanium nitride** and tungsten between an active layer of thin film transistor and an upper **layer aluminum wiring connecting** thereto.

SOLUTION: A gate oxide film 103 and a gate electrode 104 are formed on a silicon active layer 102 on a substrate 101, and impurities are selectively doped and a source area 105, a channel-forming area 106, and a drain-forming area 107 are formed (A). The gate oxide film is provided with an opening; a tungsten film is formed on whole surface of the substrate; a **titanium nitride** film is formed thereon successively; and a barrier metal 108 or a lower **layer wiring** 109 is made by dry-etching-processing the laminated layer of tungsten and **titanium nitride**. And, an **interlayer insulating film** 110 is formed thereon, and an upper part of the lower **layer wiring** 109, etc., is removed and further aluminum is formed to form an upper **layer wiring** 111 (B).

23/3,AB/14 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05004681
METHOD FOR MANUFACTURING CONNECTION HOLE

PUB. NO.: 07-297281 [JP 7297281 A]
PUBLISHED: November 10, 1995 (19951110)
INVENTOR(s): AKIBA NAMISATO
KADOMURA SHINGO
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-107692 [JP 94107692]
FILED: April 22, 1994 (19940422)

ABSTRACT

PURPOSE: To improve coverage when forming a film and to enhance yield of a **multilayer wiring** process by preventing a re-deposit from being adhering the side wall of a hole when forming a connection hole leading to a lower-**layer wiring** at an **insulation film** by etching.

CONSTITUTION: After forming a **wiring film** 12 consisting of **aluminum** metal, an etching stop film 13 consisting of **titanium nitride** or **titanium nitride** oxide by a substance succeeding to the orientation of aluminum metal and having (111) orientation is formed without exposing the surface to oxidation atmosphere and further a reflection prevention film 14 is formed. Then, those films are subjected to patterning and a wire 15 is formed. Then, after an **insulation film** 16 is formed to a state for covering the **wiring** 15, a **connection** hole 19 is formed at the **insulation film** 16 on the **wiring** 15.

23/3,AB/15 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

03945958
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE **WIRING CONNECTION** STRUCTURE AND MANUFACTURE THEREOF

PUB. NO.: 04-311058 [JP 4311058 A]
PUBLISHED: November 02, 1992 (19921102)
INVENTOR(s): HARADA SHIGERU
ISHIMARU KAZUHIRO
HAGI KIMIO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-076544 [JP 9176544]
FILED: April 09, 1991 (19910409)
JOURNAL: Section: E, Section No. 1337, Vol. 17, No. 145, Pg. 13, March 24, 1993 (19930324)

ABSTRACT

PURPOSE: To realize a stable contact at a connection hole by a method wherein a laminated film composed of a titanium layer and a titanium compound layer is used as the base **film** of an upper aluminum **wiring layer** which comes into contact with a surface layer formed on the surface of a lower **aluminum wiring layer** through the intermediary of a connection hole.

CONSTITUTION: A first **aluminum wiring layer** 4 is formed on a semiconductor board 1, and furthermore a tungsten film 312 and an interlaminar **insulating film** 5 are formed thereon. A second **aluminum wiring layer** 100 is formed on the interlaminar **insulating film** 5 to come into electrical contact with the first **aluminum wiring layer** 4 through the intermediary of a connection hole 6 bored in the film 5 so as to reach to the surface of the tungsten **film** 312. The second aluminum **wiring layer** 100 is composed of a titanium film 101 as a base **film**, **titanium nitride film** 102, and an **aluminum film** 103. As the **titanium nitride** film 102 small in reactivity with aluminum is formed on the titanium film 101, the titanium film 101 is prevented from reacting with the **aluminum film** 103.

23/3,AB/16 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

03677427
FORMING METHOD FOR METAL **WIRING LAYER**

PUB. NO.: 04-042527 [JP 4042527 A]
PUBLISHED: February 13, 1992 (19920213)
INVENTOR(s): MUKAI RYOICHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-150812 [JP 90150812]
FILED: June 08, 1990 (19900608)
JOURNAL: Section: E, Section No. 1207, Vol. 16, No. 227, Pg. 43, May 26, 1992 (19920526)

ABSTRACT

PURPOSE: To reduce the contact resistance of one layer by interposing a conductive film nonreactive with semiconductor and a wiring material at a melting temperature of a **wiring** material **film** to become a metal **wiring layer** in a boundary between a semiconductor substrate exposed in a contact hole and the **wiring layer connected** thereto.

CONSTITUTION: A contact hole 4 for exposing an n(sup +) type impurity diffused region 2 is formed in an **interlayer insulating film** 3. Then, **titanium nitride** (TiN) film 5 of a nonreactive film is deposited on the film 3 including the inner surface of the hole 4, and an **Al film** 6 is deposited thereon. A laser beam (LB) sequentially scans the film 6 while moving a substrate, the film 6 is sequentially melted, moved, Al is buried in the hole 4, and the film 6 at the upper part of the hole 4 is formed in plane with the surface of the film 6 on the layer 3. Then, the film 6 and the film 5 formed thereunder are simultaneously patterned in a wiring pattern shape, led from the region 2 to the **film** 3, and an Al **wiring layer** 6L buried flatly in the hole 4 with Al is formed.

23/3,AB/17 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

03054623
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 02-030123 [JP 2030123 A]
PUBLISHED: January 31, 1990 (19900131)
INVENTOR(s): OZAKI JUN
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-181011 [JP 88181011]
FILED: July 19, 1988 (19880719)
JOURNAL: Section: E, Section No. 915, Vol. 14, No. 178, Pg. 22, April 10, 1990 (19900410)

ABSTRACT

PURPOSE: To eliminate the occurrence of an undercut as is formed at the time of etching of a conventional two-layer film, to eliminate a disconnection and an increase in resistance of a wiring part and to enhance the reliability of a device by a method wherein a conductive film of a lower layer is left only in an opening formed in an **insulating film** and a conductive film of an upper layer formed on the lower layer conductive film is etched as a single layer **film** to form the **wiring** part.

CONSTITUTION: An opening 10 is formed in an **insulating film** 2 formed on a semiconductor substrate 1 and after that, a lower layer conductive film 3 and a coating film 5 are formed in order and the film 5 is etched to leave the film 5 only in the opening 10. Then, the film 3 is etched using the film 5 left the opening 10 as a mask to leave the film 3 only in the opening 10. Then, the film 5 is removed and after that, an upper conductive film 4 is formed on the whole surface including the upper part of the film 3 in the opening 10 and the film 4 is patterned to form a **wiring** part to **connect** to the film 3 in the opening 10. For example, said film 3 is formed of a **titanium nitride** film 1, the film 5 is formed of a photoresist 5 for flattening use and the film 4 is formed on an **Al film**.

23/3,AB/18 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

02206869
SEMICONDUCTOR DEVICE

PUB. NO.: 62-123769 [JP 62123769 A]
PUBLISHED: June 05, 1987 (19870605)
INVENTOR(s): HAMASHIMA TOSHIKI
NAKAJIMA HIDEHARU
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-263394 [JP 85263394]
FILED: November 22, 1985 (19851122)
JOURNAL: Section: E, Section No. 555, Vol. 11, No. 343, Pg. 77, November 10, 1987 (19871110)

ABSTRACT

PURPOSE: To reduce contact resistance and obtain an excellent ohmic contact for either of an N(sup +) type diffused layer or of a P(sup +) type diffused layer by making the surface concentration of the diffused layer which is **connected** to a **wiring layer** through a **titanium nitride** layer higher than a predetermined value.

CONSTITUTION: An N(sup +) type or P(sup +) type diffused layer 2 formed in a semiconductor substrate 1 is exposed in an aperture 4 provided in an **insulating layer** 3. The 1st barrier layer 4 made of Ti, PtSi or the like is formed on the surface of the exposed diffused layer 2 and the 2nd barrier layer 5 made of TiN is formed on the **layer** 4. Then a wiring **layer** 6 made of **Al** or the like is connected to the diffused layer 2 through the barrier layers 4 and 5. The surface concentration of the diffused layer 2 is controlled to be higher than 1.0X10(sup 20)cm(sup -3) by increase of dosage or employing short period annealing.

23/3,AB/19 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

01436750
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 59-148350 [JP 59148350 A]
PUBLISHED: August 25, 1984 (19840825)
INVENTOR(s): FUJITA ICHIRO
OTAKE HIDEAKI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-023502 [JP 8323502]
FILED: February 14, 1983 (19830214)
JOURNAL: Section: E, Section No. 286, Vol. 08, No. 281, Pg. 42, December 21, 1984 (19841221)

ABSTRACT

PURPOSE: To obtain a conductive film of high reliability with good efficiency by adhering an **aluminum film** on a substrate, adhering a **titanium nitride** thin **film**, and changing said **films** into a **wiring layer** by patterning.

CONSTITUTION: The first **aluminum film** 12 is adhered on the semiconductor substrate 11, and further the **titanium nitride** thin film 13 is formed. The thin **film** 13 and the **aluminum film** 12 are selectively dry-etched and thus patterned, resulting in the formation of the **wiring layer**. After forming an insulation **film** 14 on this **wiring layer**, a desired **connection** window 15 is selectively etched, and said films 14 and 13 are removed. An **aluminum wiring layer** 16 is adhered over the entire surface by a sputtering method, and a resist film 17 is applied.

25/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015310210
WPI Acc No: 2003-371144/200335
XRAM Acc No: C03-098333
XRPX Acc No: N03-296019

Manufacture of semiconductor device having wiring, by forming conductive pattern through forming **wiring** grooves on **insulating film**, and forming barrier metal **layer** and **wiring** material **layer** on conductor pattern

Patent Assignee: SONY CORP (SONY); NAGASHIMA N (NAGA-I)
Inventor: NAGASHIMA N

Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030022482	A1	20030130	US 2002157402	A	20020529	200335	B
KR 2002092203	A	20021211	KR 200230181	A	20020530	200335	
JP 2002359244	A	20021213	JP 2001164672	A	20010531	200335	

Priority Applications (No Type Date): JP 2001164672 A 20010531
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030022482	A1		6	H01L-021/44	
KR 2002092203	A			H01L-021/28	
JP 2002359244	A		5	H01L-021/3205	

Abstract (Basic): US 20030022482 A1
Abstract (Basic):

NOVELTY - A semiconductor device having wiring is manufactured by:

(i) forming a conductor pattern through forming wiring grooves on an **insulating film**; and

(ii) forming a barrier metal **layer** and a **wiring** material **layer** on the conductor pattern.

DETAILED DESCRIPTION - Manufacture of semiconductor device having wiring, comprises:

(a) forming a conductor pattern by forming wiring grooves (3a, 3b) on an **insulating film** (1, 2);

(b) forming a first barrier metal **layer** and a **wiring** material **layer** on the conductor pattern;

(c) forming a second barrier metal layer, so that a height of a surface of the barrier metal layer on protuberances of the conductor pattern is made equal or approximately equal to a height of the surface of the second barrier metal, on recesses of the conductor pattern;

(d) removing the second barrier metal layer on the protuberances of the conductor pattern;

(e) removing the **wiring** material **layer** on the protuberances of the conductor pattern; and

(f) removing the first barrier metal layer on the protuberances of the conductor pattern and the second barrier metal layer on the recesses of the conductor pattern.

USE - For manufacture of semiconductor device having wiring.

ADVANTAGE - The method provides semiconductor device, which forms **wiring** having uniform **film** thickness. It provides **wiring** of a wide line width as well as a pad, improving an increased convenience of designing circuitry, and avoiding problems

such as delay due to increase of wiring resistance.

DESCRIPTION OF DRAWING(S) - The figure is a schematic diagram illustrating a wiring groove forming process.

Insulating film (1, 2)

Wiring grooves (3a, 3b)

pp; 6 DwgNo 1A/2

25/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014212587
WPI Acc No: 2002-033284/200204
Related WPI Acc No: 1998-398068; 1999-009304; 2003-102345
XRAM Acc No: C02-009276
XRPX Acc No: N02-025543
Providing of void in spacing between wiring lines of semiconductor substrate, involves depositing conductive layers on the substrate, and subsequently configuring the conductive **layers** into adjacent **wiring** lines
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: GIVENS J H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6309946	B1	20011030	US 95550916	A	19951031	200204	B
			US 96723263	A	19960930		
			US 98207890	A	19981208		

Priority Applications (No Type Date): US 95550916 A 19951031; US 96723263 A 19960930; US 98207890 A 19981208
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6309946	B1		11	H01L-021/76	Div ex application US 95550916 Cont of application US 96723263 Cont of patent US 5835987

Abstract (Basic): US 6309946 B1
Abstract (Basic):

NOVELTY - A void between wiring lines of semiconductor substrate is provided by depositing conductive layers on the substrate; subsequently configuring the conductive **layers** to adjacent **wiring** lines; depositing a dielectric material on the substrate; and accumulating the dielectric material between edges of the extending tops of the wiring lines to seal off an elongated void area.

DETAILED DESCRIPTION - Providing void (32) in a spacing between wiring lines (34, 36, 74, 76) of semiconductor substrate involves depositing at least three conductive layers on the substrate comprising lower, middle, and an upper layer; subsequently configuring the conductive layers into at least two adjacent wiring lines, forming the lower and the middle layers to each have a lateral width less than a lateral width of the upper layer so that at least two adjacent elongated wiring lines each have a cross-sectional shape of a T, and laterally extending tops on the length of the two adjacent wiring lines; depositing dielectric material (86) on the substrate and the semiconductor at least two adjacent elongated wiring lines with the extending tops to form a **layer**; and causing the **dielectric** material to accumulate between edges of the laterally extending tops of the at least two wiring lines to seal off an elongated void area between the two elongated wiring lines.

USE - For providing void in spacing or for reducing the resistance capacitance (RC) delay between adjacent wiring lines of a semiconductor substrate.

ADVANTAGE - The method minimizes resistance-capacitance coupling.

It provides void having low dielectric value of 1.0, or reduced line spacing, e.g. less than 1 or less than 0.5 microns. It provides line spacing that is as low as 0.1 microns. The controllably defined void(s) reduce the dielectric value in the spacing between adjacent wiring lines, thus reducing RC delay.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of the planarized substrate.

Void (32)

Wiring lines (34, 36, 74, 76)

Dielectric material (86)

pp; 11 DwgNo 13/13

25/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014211289
WPI Acc No: 2002-031986/200204
XRAM Acc No: C02-008929
Method for forming metal line
Patent Assignee: HYNIX SEMICONDUCTOR INC (HYNI-N)
Inventor: CHOI C J; KIM Y C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001063782	A	20010709	KR 9961870	A	19991224	200204	B

Priority Applications (No Type Date): KR 9961870 A 19991224
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001063782	A		1	H01L-021/28	

Abstract (Basic): KR 2001063782 A
Abstract (Basic):
NOVELTY - A method for forming a metal line is provided to improve the reliability wiring by forming a plug layer after forming a metal line layer.
DETAILED DESCRIPTION - An **interlayer dielectric**(32), a **wiring layer**(34), and a hard mask layer(35) are formed on a substrate(31). A contact hole for exposing the substrate(31) is formed by etching selectively the hard mask **layer**(35), the wiring **layer**(34), and the **interlayer dielectric**(32). A plug **layer** is formed within the contact hole. The substrate(31) is **connected** with the **wiring layer** by the plug **layer**. The **wiring layer**(34) is formed by laminating a **titanium/titanium nitride** layer(33) of 300 to 1000 angstrom and an **aluminium layer**(34) of 3000 to 10000 angstrom.
pp; 1 DwgNo 1/10

25/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012870806
WPI Acc No: 2000-042639/200004
XRAM Acc No: C00-011885
XRPX Acc No: N00-032289
Contact hole formation procedure in semiconductor device manufacture - involves embedding tungsten only in connection hole by chemical vapor deposition, after which **wiring layer** having **aluminum** alloy is formed
Patent Assignee: SEIKO EPSON CORP (SHIH)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11297822	A	19991029	JP 9897997	A	19980409	200004	B

Priority Applications (No Type Date): JP 9897997 A 19980409
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11297822	A		6	H01L-021/768	

Abstract (Basic): JP 11297822 A

NOVELTY - A **titanium nitride** layer (104) and is formed on **insulating film** (103) on silicon substrate. A connection hole (106) is formed on TiN **layer** (104) and **insulating film** (103). Then, tungsten (107) is embedded only in connection hole by chemical vapor deposition, after which **wiring layer** having **aluminum** alloy (108) is formed.

USE - In semiconductor device manufacture.

ADVANTAGE - As connection hole is formed after formation of **titanium nitride** layer, **titanium nitride** do not exist in the side wall of connection hole or via hole. Moreover when patterning aluminum alloy to produce eye gap is performed, a microgroove is not generated in the **connection** hole, hence **wiring** with high yield and reliability is obtained.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of semiconductor device manufacturing method. (103) **Insulating film**; (104) **Titanium nitride** layer; (106) Connection hole; (107) Tungsten; (108) Aluminum alloy.

Dwg.1/3

25/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011922473
WPI Acc No: 1998-339383/199830
XRPX Acc No: N98-265587
Semiconductor device manufacturing method - involves forming main **wiring layer** made of **aluminium** system material, on surface of thin base film embedding inside connection hole, by sputtering technique at high temperature
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10125778	A	19980515	JP 96275693	A	19961018	199830	B

Priority Applications (No Type Date): JP 96275693 A 19961018
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10125778	A		5	H01L-021/768	

Abstract (Basic): JP 10125778 A

The method involves forming a double layered barrier metal film (36) on the inner wall of a connection hole (33) formed in an **insulating film** (32) over a substrate (31), and as well as on the **insulating film**. A thin base film (10) is formed on the entire surface of the barrier metal film including in the connection hole, by sputtering process at a low temperature to prevent flow of film-forming substance.

The thin base **film** is made of **aluminium** system material or copper system material. The thin base film offers high wettability than a **titanium-nitride** layer (35) which is the surface layer of the barrier metal **film**. A main wiring **layer** (11) made of **aluminium** system material is formed on the surface of the thin base film, thereby embedding inside the connection hole, by sputtering technique at high temperature.

ADVANTAGE - Secures **connection** state of **wirings**. Improves reliability of semiconductor device.

Dwg.1/5

25/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011922392
WPI Acc No: 1998-339302/199830
XRPX Acc No: N98-265506
Semiconductor device with multilayered interconnection structure manufacturing method - involves interposing sublayer wiring containing **titanium** and **titanium nitride** between upper and lower **aluminium** alloy **layer**
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10125679	A	19980515	JP 96277783	A	19961021	199830	B

Priority Applications (No Type Date): JP 96277783 A 19961021
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10125679	A		9	H01L-021/3205	

Abstract (Basic): JP 10125679 A
The method involves forming an **insulating film** (12) on a semiconductor substrate (11). A sublayer wiring (14,15) containing **titanium** and **titanium nitride**, is interposed between upper and lower **aluminium** alloy **layer** (13,16).
The upper **aluminium** alloy **layer** is covered by an **interlayer insulating film** (18). A through-hole (19) is formed in the **interlayer insulating film**, in which a metal plug (21) is inserted, so that first and second **wiring layers** are electrically **connected** by the metal plug.
ADVANTAGE - Improves electromigration resistance. Prolongs substantial element life. Prevents disconnection and inferior connection.
Dwg.1/7

25/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011865399
WPI Acc No: 1998-282309/199825
XRAM Acc No: C98-087455
XRPX Acc No: N98-222843
Implanting wiring pattern formation method for semiconductor device e.g. LSIC - involves forming upper **aluminium** alloy **wiring layer** on **titanium nitride** film, such that its thickness is more than three times of width of **wiring** groove formed on **interlayer insulating film**
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10098039	A	19980414	JP 96271787	A	19960920	199825	B

Priority Applications (No Type Date): JP 96271787 A 19960920
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10098039	A		11	H01L-021/3205	

Abstract (Basic): JP 10098039 A

The method involves forming an **interlayer insulating film** (3) on surface of substrate. A connection hole (4), and a wiring groove (5) are formed in the **interlayer insulating film** at predetermined position. A **titanium nitride** film (6) is formed on the **interlayer insulating film**. An upper **Al**-alloy **wiring layer** (7) is formed on the entire surface of the substrate with thickness more than three times the width of the wiring groove. A bridge shape is formed on portion of **wiring** groove and **connection** hole. For formation of the bridge shape, a dummy pattern is formed near **connection** area of **wiring** groove and **connection** hole.

Then, high pressure reflow process is performed under inert gas environment thereby Al-alloy is filled up into the **wiring** groove and the **connection** hole. Then, the **interlayer insulating film** is subjected to chemo-mechanical polishing process. Thereby implanting wiring is formed inside the wiring groove.

ADVANTAGE - Facilitates formation of implanting wiring with high stability. Facilitates formation of bridge shape on portion of wiring groove with high stability.

Dwg.2/22

25/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011519344
WPI Acc No: 1997-495830/199746
XRAM Acc No: C97-157794
XRPX Acc No: N97-412994

Multilayered wiring structure formation for semiconductor device - involves using mixed gas to etch **interlayer insulating film** and **titanium nitride** film to form **connection** hole of **wiring** structure

Patent Assignee: NEC KYUSHU LTD (KYUN)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9232424	A	19970905	JP 9633888	A	19960221	199746	B

Priority Applications (No Type Date): JP 9633888 A 19960221
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9232424	A		5	H01L-021/768	

Abstract (Basic): JP 9232424 A

The method involves forming a wiring structure having a TiN film (3) as the upper most layer on a Si substrate (20). An **interlayer insulating film** (2) surmounts the upper surface of the substrate.

A connection hole is formed on **Al**-Si-Cu **film** (4) of the **wiring** structure, by etching the **interlayer insulating film** and the TiN film using the fluoro carbon group gas like CF4 and CHF3. To promote etching of TiN film, SF6, He and N2 are mixed to the fluorocarbon group gases.

ADVANTAGE - Improves reliability and speed electromigration. Prevents stress migration policy.

Dwg.1/3

25/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010777907
WPI Acc No: 1996-274860/199628
Related WPI Acc No: 2003-347366
XRAM Acc No: C96-087187
XRPX Acc No: N96-231246

Forming multilayer interconnection for semiconductor device - involves forming **aluminium@ wiring layer, titanium@ layer** as **nitride** barrier, **titanium nitride** anti-reflection **layer** and **interlayer insulating layer**

Patent Assignee: YAMAHA CORP (NIHG)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8115979	A	19960507	JP 94276046	A	19941014	199628	B

Priority Applications (No Type Date): JP 94276046 A 19941014
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8115979	A		5	H01L-021/768	

Abstract (Basic): JP 8115979 A

The method involves forming a lower part **wiring layer** (32a) which consists of an **aluminium** alloy **film** (14b), a **Ti** film for **nitride** prevention (14c) and a TiN film for a reflected prevention (14d). An **interlayer insulating film** (34) is formed hiding the lower part **wiring layer** by selection etching process using a resist layer as a mask.

The resist layer is then removed. The lower part **wiring layer** is **connected** to an upper part **wiring layer** through the **connection** hole. The base of the connection hole is then positioned in the TiN film.

ADVANTAGE - Reduces connection resistance of interlayer connection part. Reduces variation in connection resistance. Improves yield.

Dwg.4/9

25/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010528556
WPI Acc No: 1996-025509/199603
XRAM Acc No: C96-008451
XRPX Acc No: N96-021644

Mfr. of connection hole for highly integrated semiconductor device - comprises forming **aluminium wiring layer**, patterning by etching, and forming the connection hole in **insulating layer** deposited on **wiring layer**

Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7297281	A	19951110	JP 94107692	A	19940422	199603	B

Priority Applications (No Type Date): JP 94107692 A 19940422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7297281	A		7	H01L-021/768	

Abstract (Basic): JP 7297281 A

The connection hole mfg. method is applicable to a substance (11), on which a **wiring** metal **layer** (12) of **Al** system is formed. Surface of **wiring layer** is exposed to the oxidising environment. An etching stop layer of TiN or **Ti** oxide **nitride** system is formed on the **wiring layer**. A non-reflecting film (14) is formed on the etching stop layer.

Patterning of the **wiring layer**, the etching stop layer and the reflected prevention layer is carried out to form the wiring structure (15). An **insulating film** (16) if formed on the **wiring layer**. A **connection** hole (19) is formed on the wiring structure.

ADVANTAGE - Obtains high etching selection ratio. Reduces time required for film formation. Improves reliability during wiring process. Improved yield. Reduces chip area and cost of mfr..

Dwg.1/4

25/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010233445
WPI Acc No: 1995-134702/199518
XRAM Acc No: C95-061998
XRPX Acc No: N95-106037

Multilayer interconnection structure of semiconductor devices e.g. LSI - uses second **wiring layer connected** to first **wiring layer** through **connection** hole with **titanium nitride** film at hole's bottom

Patent Assignee: YAMAHA CORP (NIHG)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7058110	A	19950303	JP 93219069	A	19930811	199518	B

Priority Applications (No Type Date): JP 93219069 A 19930811
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7058110	A		6	H01L-021/3205	

Abstract (Basic): JP 7058110 A

The structure is formed by an **insulating film** (14) hiding the surface of a semiconductor substrate (10). A connection hole (14A) is formed on the **insulating film**. A **wiring layer** (16) is formed to the **insulating film**, which is connected to the substrate. An **interlayer** insulating **film** (18) covers the **wiring layer** and the **insulating film**. The **wiring layer** is composed of a Ti **film** (16a), a TiON **film** (16b), an **Al film** (16c), a Ti film (16d) and a TiN film (16e). The setup is heat treated in a temperature ranging from 400-500 degree centigrade for 30 minutes. A connection hole (18A) is formed, with the TiN film as bottom (Z) of the second **connection** hole. A second **wiring layer** (20) is **connected** to the first **wiring layer**, through the second connection hole.

ADVANTAGE - Improves connection state of interlayer connection part; reduces junction leak current; and inhibits generation of aluminium hillocks and alloy pits.

Dwg.1/7

25/3,AB/12 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06262945
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 11-204526 [JP 11204526 A]
PUBLISHED: July 30, 1999 (19990730)
INVENTOR(s): SHINOMIYA HIDEO
SUGIMOTO SHIGEKI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 10-006240 [JP 986240]
FILED: January 16, 1998 (19980116)

ABSTRACT

PROBLEM TO BE SOLVED: To decrease the electrical resistance of a connecting hole by thinning the thickness of a film, which is deposited in the connecting hole by providing a metal **wiring**, the **connecting** hole which is formed to the upper surface of the metal wiring from the upper surface of a conducting film, a lubricating film, which facilitates the formation of the **wiring** in the **connecting** hole, and the like.

SOLUTION: Aluminum 34 which is used as a metal wiring is formed. A silicon dioxide film 35 is formed as the **interlayer insulating film** so as to embed the **aluminum** on the **insulating film**. A titanium **film** 36 is formed as a lubricating film on the upper surface of the silicon dioxide film 35. Furthermore, a **titanium nitride** film 37 is formed as the conducting film on the upper surface of the titanium film 36. Then, a connecting hole 38, which reaches the upper surface of the aluminum 34 from the upper surface of the **titanium nitride** film 37 is formed at a specified position. Aluminum 40, which becomes the second wiring, is formed on the entire surface on the **titanium nitride** 37. The **titanium nitride film** 37 prevents the **wire** breakdown of the aluminum 40 and improves the directivity of the aluminum 40. Furthermore, a titanium film 39 facilitates the in flow of the aluminum 40 into the connecting hole 38.

25/3,AB/13 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05971283
SEMICONDUCTOR DEVICE AND ORGANIC EL DISPLAY DEVICE

PUB. NO.: 10-254383 [JP 10254383 A]
PUBLISHED: September 25, 1998 (19980925)
INVENTOR(s): YAMAUCHI YUKIO
ARAI MICHIO
APPLICANT(s): TDK CORP [000306] (A Japanese Company or Corporation), JP (Japan)
SEMICONDUCTOR ENERGY LAB CO LTD [470730] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-053243 [JP 9753243]
FILED: March 07, 1997 (19970307)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor device, which is non-corroding and non- deteriorating, and allows a stable electric connection, reduces a specific resistance, and improves processability, by providing a barrier metal laminating **titanium nitride** and tungsten between an active layer of thin film transistor and an upper **layer aluminum wiring connecting** thereto.

SOLUTION: A gate oxide film 103 and a gate electrode 104 are formed on a silicon active layer 102 on a substrate 101, and impurities are selectively doped and a source area 105, a channel-forming area 106, and a drain-forming area 107 are formed (A). The gate oxide film is provided with an opening; a tungsten film is formed on whole surface of the substrate; a **titanium nitride** film is formed thereon successively; and a barrier metal 108 or a lower **layer wiring** 109 is made by dry-etching-processing the laminated layer of tungsten and **titanium nitride**. And, an **interlayer insulating film** 110 is formed thereon, and an upper part of the lower **layer wiring** 109, etc., is removed and further aluminum is formed to form an upper **layer wiring** 111 (B).

25/3,AB/14 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05004681
METHOD FOR MANUFACTURING CONNECTION HOLE

PUB. NO.: 07-297281 [JP 7297281 A]
PUBLISHED: November 10, 1995 (19951110)
INVENTOR(s): AKIBA NAMISATO
KADOMURA SHINGO
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-107692 [JP 94107692]
FILED: April 22, 1994 (19940422)

ABSTRACT

PURPOSE: To improve coverage when forming a film and to enhance yield of a **multilayer wiring** process by preventing a re-deposit from being adhering the side wall of a hole when forming a connection hole leading to a lower-**layer wiring** at an **insulation film** by etching.

CONSTITUTION: After forming a **wiring film** 12 consisting of **aluminum** metal, an etching stop film 13 consisting of **titanium nitride** or **titanium nitride** oxide by a substance succeeding to the orientation of aluminum metal and having (111) orientation is formed without exposing the surface to oxidation atmosphere and further a reflection prevention film 14 is formed. Then, those films are subjected to patterning and a wire 15 is formed. Then, after an **insulation film** 16 is formed to a state for covering the **wiring** 15, a **connection** hole 19 is formed at the **insulation film** 16 on the **wiring** 15.

25/3,AB/15 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

03945958
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE **WIRING CONNECTION** STRUCTURE AND MANUFACTURE THEREOF

PUB. NO.: 04-311058 [JP 4311058 A]
PUBLISHED: November 02, 1992 (19921102)
INVENTOR(s): HARADA SHIGERU
ISHIMARU KAZUHIRO
HAGI KIMIO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-076544 [JP 9176544]
FILED: April 09, 1991 (19910409)
JOURNAL: Section: E, Section No. 1337, Vol. 17, No. 145, Pg. 13, March 24, 1993 (19930324)

ABSTRACT

PURPOSE: To realize a stable contact at a connection hole by a method wherein a laminated film composed of a titanium layer and a titanium compound layer is used as the base **film** of an upper aluminum **wiring layer** which comes into contact with a surface layer formed on the surface of a lower **aluminum wiring layer** through the intermediary of a connection hole.

CONSTITUTION: A first **aluminum wiring layer** 4 is formed on a semiconductor board 1, and furthermore a tungsten film 312 and an interlaminar **insulating film** 5 are formed thereon. A second **aluminum wiring layer** 100 is formed on the interlaminar **insulating film** 5 to come into electrical contact with the first **aluminum wiring layer** 4 through the intermediary of a connection hole 6 bored in the film 5 so as to reach to the surface of the tungsten **film** 312. The second aluminum **wiring layer** 100 is composed of a titanium film 101 as a base **film**, **titanium nitride film** 102, and an **aluminum film** 103. As the **titanium nitride** film 102 small in reactivity with aluminum is formed on the titanium film 101, the titanium film 101 is prevented from reacting with the **aluminum film** 103.

25/3,AB/16 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

03677427
FORMING METHOD FOR METAL **WIRING LAYER**

PUB. NO.: 04-042527 [JP 4042527 A]
PUBLISHED: February 13, 1992 (19920213)
INVENTOR(s): MUKAI RYOICHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-150812 [JP 90150812]
FILED: June 08, 1990 (19900608)
JOURNAL: Section: E, Section No. 1207, Vol. 16, No. 227, Pg. 43, May 26, 1992 (19920526)

ABSTRACT

PURPOSE: To reduce the contact resistance of one layer by interposing a conductive film nonreactive with semiconductor and a wiring material at a melting temperature of a **wiring** material **film** to become a metal **wiring layer** in a boundary between a semiconductor substrate exposed in a contact hole and the **wiring layer connected** thereto.

CONSTITUTION: A contact hole 4 for exposing an n(sup +) type impurity diffused region 2 is formed in an **interlayer insulating film** 3. Then, **titanium nitride** (TiN) film 5 of a nonreactive film is deposited on the film 3 including the inner surface of the hole 4, and an **Al film** 6 is deposited thereon. A laser beam (LB) sequentially scans the film 6 while moving a substrate, the film 6 is sequentially melted, moved, Al is buried in the hole 4, and the film 6 at the upper part of the hole 4 is formed in plane with the surface of the film 6 on the layer 3. Then, the film 6 and the film 5 formed thereunder are simultaneously patterned in a wiring pattern shape, led from the region 2 to the **film** 3, and an Al **wiring layer** 6L buried flatly in the hole 4 with Al is formed.

25/3,AB/17 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

03054623
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 02-030123 [JP 2030123 A]
PUBLISHED: January 31, 1990 (19900131)
INVENTOR(s): OZAKI JUN
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-181011 [JP 88181011]
FILED: July 19, 1988 (19880719)
JOURNAL: Section: E, Section No. 915, Vol. 14, No. 178, Pg. 22, April 10, 1990 (19900410)

ABSTRACT

PURPOSE: To eliminate the occurrence of an undercut as is formed at the time of etching of a conventional two-layer film, to eliminate a disconnection and an increase in resistance of a wiring part and to enhance the reliability of a device by a method wherein a conductive film of a lower layer is left only in an opening formed in an **insulating film** and a conductive film of an upper layer formed on the lower layer conductive film is etched as a single layer **film** to form the **wiring** part.

CONSTITUTION: An opening 10 is formed in an **insulating film** 2 formed on a semiconductor substrate 1 and after that, a lower layer conductive film 3 and a coating film 5 are formed in order and the film 5 is etched to leave the film 5 only in the opening 10. Then, the film 3 is etched using the film 5 left the opening 10 as a mask to leave the film 3 only in the opening 10. Then, the film 5 is removed and after that, an upper conductive film 4 is formed on the whole surface including the upper part of the film 3 in the opening 10 and the film 4 is patterned to form a **wiring** part to **connect** to the film 3 in the opening 10. For example, said film 3 is formed of a **titanium nitride** film 1, the film 5 is formed of a photoresist 5 for flattening use and the film 4 is formed on an **Al film**.

25/3,AB/18 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

02206869
SEMICONDUCTOR DEVICE

PUB. NO.: 62-123769 [JP 62123769 A]
PUBLISHED: June 05, 1987 (19870605)
INVENTOR(s): HAMASHIMA TOSHIKI
NAKAJIMA HIDEHARU
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-263394 [JP 85263394]
FILED: November 22, 1985 (19851122)
JOURNAL: Section: E, Section No. 555, Vol. 11, No. 343, Pg. 77, November 10, 1987 (19871110)

ABSTRACT

PURPOSE: To reduce contact resistance and obtain an excellent ohmic contact for either of an N(sup +) type diffused layer or of a P(sup +) type diffused layer by making the surface concentration of the diffused layer which is **connected** to a **wiring layer** through a **titanium nitride** layer higher than a predetermined value.

CONSTITUTION: An N(sup +) type or P(sup +) type diffused layer 2 formed in a semiconductor substrate 1 is exposed in an aperture 4 provided in an **insulating layer** 3. The 1st barrier layer 4 made of Ti, PtSi or the like is formed on the surface of the exposed diffused layer 2 and the 2nd barrier layer 5 made of TiN is formed on the **layer** 4. Then a wiring **layer** 6 made of **Al** or the like is connected to the diffused layer 2 through the barrier layers 4 and 5. The surface concentration of the diffused layer 2 is controlled to be higher than 1.0X10(sup 20)cm(sup -3) by increase of dosage or employing short period annealing.

25/3,AB/19 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

01436750
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 59-148350 [JP 59148350 A]
PUBLISHED: August 25, 1984 (19840825)
INVENTOR(s): FUJITA ICHIRO
OTAKE HIDEAKI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-023502 [JP 8323502]
FILED: February 14, 1983 (19830214)
JOURNAL: Section: E, Section No. 286, Vol. 08, No. 281, Pg. 42, December 21, 1984 (19841221)

ABSTRACT

PURPOSE: To obtain a conductive film of high reliability with good efficiency by adhering an **aluminum film** on a substrate, adhering a **titanium nitride** thin **film**, and changing said **films** into a **wiring layer** by patterning.

CONSTITUTION: The first **aluminum film** 12 is adhered on the semiconductor substrate 11, and further the **titanium nitride** thin film 13 is formed. The thin **film** 13 and the **aluminum film** 12 are selectively dry-etched and thus patterned, resulting in the formation of the **wiring layer**. After forming an insulation **film** 14 on this **wiring layer**, a desired **connection** window 15 is selectively etched, and said films 14 and 13 are removed. An **aluminum wiring layer** 16 is adhered over the entire surface by a sputtering method, and a resist film 17 is applied.

28/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015380355
WPI Acc No: 2003-441296/200341
XRAM Acc No: C03-116777
XRPX Acc No: N03-352290
Etchant for, e.g. molybdenum, molybdenum alloy wire, comprises specified percentage of nitric acid, phosphoric acid, acetic acid, stabilizer and other ultra pure water
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KANG S; PARK H
Number of Countries: 100 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200336377	A1	20030501	WO 2002KR112	A	20020124	200341	B

Priority Applications (No Type Date): KR 200165326 A 20011023
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200336377	A1	E	65	G02F-001/136	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

Abstract (Basic): WO 200336377 A1
Abstract (Basic):
NOVELTY - An etchant for wire comprises nitric acid (0.1-10%); phosphoric acid (65-55%); acetic acid (5-20%); stabilizer (0.1-5%); and other ultra pure water.
DETAILED DESCRIPTION - An etchant for wire comprises nitric acid (0.1-10%); phosphoric acid (65-55%); acetic acid (5-20%); stabilizer (0.1-5%); and other ultra pure water. The stabilizer has a structure of formula M(OH)xLy.
M=zinc, tin, chromium, aluminum, barium, iron, titanium, silicon or boron;
L=water, NH3, CN, COR; NNR
R=1-5C alkyl;
x=2 or 3; and
y=0, 1, 2, 3.
INDEPENDENT CLAIMS are also included for:
(a) a method for manufacturing wire for display comprising depositing a first conductive film (2) of molybdenum or molybdenum alloy on a substrate; and etching the first conductive film using the etchant as above;
(b) a method of manufacturing a thin film transistor array panel comprising forming a gate wire including a gate line and a gate electrode; forming a gate insulating **layer** covering the gate **wire**; forming a semiconductor **layer** on the gate insulating layer of the gate electrode; and forming a data wire including a source electrode, a drain electrode and a data line on the semiconductor layer or the gate insulating layer; and

(c) a thin film transistor array panel, comprising a gate wire formed on an insulating substrate and including a gate line and a gate pad connected to the gate line; a gate insulating **layer** covering the gate **wire**; a semiconductor **layer** formed on the gate insulating **layer**; a data **wire** formed on the gate insulating layer or the semiconductor layer and including a data line, a source electrode connected to the data line and formed on the semiconductor layer, and a drain electrode formed on semiconductor layer disposed opposite the source electrode in relation to the gate electrode; a passivation **layer** covering the data **wire**; and a conductor pattern made of indium zinc oxide and formed in the passivation layer.

The gate wire or the data wire is formed with a first conductive film made of molybdenum or molybdenum alloy. The first conductive film is patterned using the etchant above.

USE - The etchant is used to etch molybdenum, molybdenum alloy, or molybdenum tungsten alloy, preferably molybdenum tungsten alloy (claimed).

ADVANTAGE - The inventive etchant etches wire of molybdenum or molybdenum alloy formed of a low resistant material and having low resistant contact feature with another material, to pattern the wire to provide a good taper structure and excellent evenness.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view showing an etched profile when molybdenum tungsten alloy film is etched using the etchant for wire above.

Film (2)

pp; 65 DwgNo 1/17

28/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014919157
WPI Acc No: 2002-739864/200280
XRAM Acc No: C02-209485
XRPX Acc No: N02-582866
Semiconductor device comprises wirings formed in **wiring** grooves, and **connector** formed integrally with **wirings** in via holes
Patent Assignee: HITACHI LTD (HITA)
Inventor: AOKI H; MIYAZAKI H; OHMORI K; OSHIMA T
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020100984	A1	20020801	US 2001987914	A	20011116	200280	B
KR 2002042458	A	20020605	KR 200174455	A	20011128	200280	
JP 2002164428	A	20020607	JP 2000362462	A	20001129	200280	

Priority Applications (No Type Date): JP 2000362462 A 20001129
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020100984	A1		35	H01L-021/4763	
KR 2002042458	A			H01L-021/3205	
JP 2002164428	A		24	H01L-021/768	

Abstract (Basic): US 20020100984 A1
Abstract (Basic):
NOVELTY - A semiconductor device comprises wirings formed in wiring grooves (20); and a connector formed integrally with the wirings in via holes for **connecting** the **wirings** and lower layer wirings.
The Young's modulus of the first dielectric layer in which the via holes are formed, is smaller than the Young's modulus of a second dielectric **layer** in which the **wiring** grooves are formed.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the production of the above semiconductor device comprising forming a first dielectric layer and a second dielectric layer; forming the via holes at predetermined regions of the first dielectric **layer** and forming the **wiring** grooves at predetermined regions of the second dielectric layer; and burying a conductive member inside the via holes and the wiring grooves.
USE - As a semiconductor device.
ADVANTAGE - The semiconductor device has a **multi-layered wiring** structure with a silicon oxide film that repulses strongly to the stress of copper.
DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of main portion of a semiconductor substrate showing the semiconductor device.
Wirings (14)
Via hole (16)
Stopper dielectric thin film (18)
Wiring grooves (20)
pp; 35 DwgNo 1/26

28/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014511164
WPI Acc No: 2002-331867/200237
Related WPI Acc No: 2002-331866; 2002-341991
XRAM Acc No: C02-095858
XRPX Acc No: N02-260589
Film forming method by preparing film forming gas consisting of alkoxy compound or siloxane and oxygen-containing gas, and forming silicon-containing insulating film on substrate by plasmanizing the film forming gas to react
Patent Assignee: CANON SALES CO INC (CANO); SEMICONDUCTOR PROCESS LAB CO LTD (SEMI-N); CANON HANBAI KK (CANO-N); HANDOTAI PROCESS KENKYUSHO KK (HAND-N)
Inventor: AOKI J; KOROMOKAWA T; MAEDA K; OKU T; YAMAMOTO Y
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1174915	A2	20020123	EP 2001116694	A	20010717	200237	B
JP 2002164346	A	20020607	JP 2001220232	A	20010719	200241	
KR 2002009440	A	20020201	KR 200143736	A	20010720	200254	
TW 503514	A	20020921	TW 2001117414	A	20010717	200337	

Priority Applications (No Type Date): JP 2000281263 A 20000918; JP 2000221379 A 20000721
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1174915	A2	E	33	H01L-021/316	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2002164346	A		18	H01L-021/316	
KR 2002009440	A			H01L-021/203	
TW 503514	A			H01L-021/765	

Abstract (Basic): EP 1174915 A2
Abstract (Basic):
NOVELTY - Film forming method involves:
(i) preparing a film forming gas consisting of alkoxy compound or siloxane having silicon-hydrogen bonds, and oxygen-containing gas including oxygen, nitrous oxide, nitrogen dioxide, carbon monoxide, carbon dioxide, or water; and
(ii) forming a silicon-containing insulating film on the substrate by plasmanizing the film forming gas to react.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:
(A) a semiconductor device manufacturing method which comprises preparing a substrate on a surface of which a wiring is formed, and forming a silicon-containing insulating **film** for covering the **wiring** by plasmanizing a **film** forming gas to react; and
(B) a semiconductor device in which a silicon-containing insulation film whose peak of an absorption intensity of an infrared rays is in a wave number 2270-2350/cm, whose film density is 2.25-2.4 g/cm3, and whose relative dielectric constant is 3.3-4.3, is formed on a substrate.
USE - For forming an insulating film for a semiconductor device.
ADVANTAGE - The method is capable of lowering a dielectric constant

of an interlayer insulating film as a whole and suppressing a change of the dielectric constant due to moisture absorption, while preventing corrosion of a wiring and an increase in a leakage current.

DESCRIPTION OF DRAWING(S) - The figure is a side view of a configuration of a plasma chemical vapor deposition film forming equipment employed in the inventive method.

Parallel-plate type electrodes (2, 3)

Substrate (20)

pp; 33 DwgNo 1/16

28/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014222216
WPI Acc No: 2002-042914/200206
XRPX Acc No: N02-031851
Semiconductor device interconnection structure comprising additional capacitors with capacitors formed at desired positions to make countermeasure for power source noise
Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA DENKI SANGYO KK (MATU)
Inventor: MORIWAKI T; SUZUKI R; TAMARU M
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1071130	A2	20010124	EP 2000115236	A	20000713	200206	B
JP 2001085630	A	20010330	JP 2000212973	A	20000713	200206	
KR 2001029950	A	20010416	KR 200040721	A	20000714	200206	
TW 483150	A	20020411	TW 2000114073	A	20000714	200313	

Priority Applications (No Type Date): JP 99200845 A 19990714
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1071130	A2	E	31	H01L-023/522	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2001085630	A		20	H01L-027/04	
KR 2001029950	A			H01L-027/04	
TW 483150	A			H01L-027/08	

Abstract (Basic): EP 1071130 A2
Abstract (Basic):
NOVELTY - An insulating inter-layer film of silicon dioxide is formed between the through holes (B11,B12) in a silicon substrate and a metal inter-**wiring film** of **SiOF** is formed between metallic wiring (M11,M12). When the structure is used as a supplementary capacitor to power source wiring for a countermeasure against noise, one metallic **wiring** is **connected** to the power source potential and the other to another power source potential, while the structure is formed in the area where switching noise is generated.
DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is included for a method for manufacturing a semiconductor device.
USE - Forming a capacitor at a desired position to counter power source noises.
ADVANTAGE - Forming large capacity capacitors in a smaller area.
DESCRIPTION OF DRAWING(S) - The drawing shows a portion where a capacitor of a semiconductor device is formed according to a first embodiment
Through holes (B11,B12)
Metallic wiring (M11,M12)
pp; 31 DwgNo 1a/15

28/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06597371
WIRING STRUCTURE FOR SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME

PUB. NO.: 2000-183168 [JP 2000183168 A]
PUBLISHED: June 30, 2000 (20000630)
INVENTOR(s): YASUDA MAKOTO
APPLICANT(s): NEC CORP
APPL. NO.: 10-362468 [JP 98362468]
FILED: December 21, 1998 (19981221)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a multi-step wiring structure, capable of suppressing the generation and progress of EM phenomenon of Al.

SOLUTION: This wiring structure 40 is constituted by a lower wiring 44 formed on a base insulating film 42, an interlayer insulating film 46 formed on the wiring 44, a contact 48 which penetrates the **layer** 46, an upper **wiring** 50 **connected** with the **wiring** 44 via the contact 48. The layer 44 is constituted by an Al-Cu alloy **layer** which constitutes a **wiring** main body, a Ti layer 44b, and a TiN layer 44c. The layer 46 is constituted of a BPSG film 46a and an **SiOF** film 46b. The layer 50 is arranged between a contact and is constituted by a laminated barrier metal layer 52 having high (111) orientability, an Al-Cu alloy **layer** 50a constituting the **wiring** main body, a Ti layer 50b and a TiN layer 50c. The barrier metal layer 52 having high (111) orientability is constituted of a Ti layer 52a, having a film thickness of 20 nm and the TiN layer 52b the thickness of 40 nm for improving the (111) orientability and to suppress the generation and progress of EM phenomenon of Al.

28/3,AB/6 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06170298
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-111845 [JP 11111845 A]
PUBLISHED: April 23, 1999 (19990423)
INVENTOR(s): MATSUNOU TADASHI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 09-271134 [JP 97271134]
FILED: October 03, 1997 (19971003)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor device which can suppress impurity diffusion and infiltration of water or hydroxyl ions for improving its reliability.

SOLUTION: Formed on an element isolation insulating **film** 11 is a **wiring layer** 20 of a plurality of first metal wiring lines. Formed on the insulating film 11 and the first metallic **wiring layer** 20 are a silicon oxide film 31 added in high concentration of fluorine, a silicon nitride film 32 and an SiO2 film 33. The SiO2 film 33 higher in relative permittivity than the **SiOF** film 31 but lower than that of the silicon nitride film 32. Formed, in the **SiOF** film 31, silicon nitride film 32 and SiO2 film 33 is a via hole for **connection** with the first **wiring layer** 20. A W plug material 41 is embedded in the via hole. A second metal **wiring layer** 50 is formed on the SiO2 film 33.

28/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06020198
MULTILAYERED INTERCONNECTION STRUCTURE AND ITS FORMING METHOD

PUB. NO.: 10-303298 [JP 10303298 A]
PUBLISHED: November 13, 1998 (19981113)
INVENTOR(s): YOKOYAMA KOJI
YAMADA YOSHIAKI
KISHIMOTO KOJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-109291 [JP 97109291]
FILED: April 25, 1997 (19970425)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a multilayered interconnection structure which has an **SiOF** film as an interlayer insulating film, the excellent flatness and the high reliability by a method wherein an oxide film which does not contain fluorine and whose surface is levelled is formed on an oxide film which contains fluorine and fills the spaces between a plurality of **wiring layers** formed on a semiconductor substrate.

SOLUTION: 1st **wiring layers** 4 are formed on a semiconductor substrate with an insulating film therebetween. An **SiOF** film 6 containing fluorine and an intermediate insulating film 7 which does not contain fluorine are formed, and an SOG film 8 is formed and its surface is levelled. The surfaces of the SOG film 8 and the intermediate insulating film 7 are etched back by fluorine system gas, through-holes are formed at predetermined positions, and 2nd **wiring layers** electrically connected to the 1st **wiring layers** are formed. The intermediate insulating layer 7 improves the precision of the etching back using a levelled film such as the SOG film 8. Further, the penetration of moisture into the **SiOF** film 6 which has a high moisture absorption property is avoided. The increase of the dielectric constant of the **SiOF** film 6 can be avoided and the corrosion of a through-hole part wiring caused by moisture can be eliminated.

32/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5240013 INSPEC Abstract Number: B9605-0520F-087
Title: Properties of fluorinated silicon oxide films formed using fluorotriethoxysilane for interlayer dielectrics in multilevel interconnections
Author(s): Homma, T.
Author Affiliation: ULSI Device Dev. Lab., NEC Corp., Sagamihara, Japan
Journal: Journal of the Electrochemical Society vol.143, no.3 p. 1084-7
Publisher: Electrochem. Soc,
Publication Date: March 1996 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
SICI: 0013-4651(199603)143:3L.1084:PFSO;1-C
Material Identity Number: J010-96003
U.S. Copyright Clearance Center Code: 0013-4651/96/$7.00
Language: English
Abstract: Properties of a fluorinated silicon oxide (**SiOF**) film for interlayer dielectrics in multilevel interconnections of ultralarge-scale integrated circuits (ULSIs) are investigated. The **SiOF** films are formed by a room temperature chemical vapor deposition (RTCVD) technique using fluorotriethoxysilane [FSi(OC/sub 2/H/sub 5/)/sub 3/, FTES] and pure water as gas sources. The **SiOF** film property changes by annealing at 400 or 900 degrees C are studied. Although the Si-O bond absorption peak position in the Fourier transform infrared (FTIR) spectrum is not changed by 400 degrees C annealing, the peak position for the 900 degrees C annealed **SiOF** films shifts to low wave numbers. The full width at half-maximum (FWHM) of the Si-O bond absorption peak increases by 400 degrees C annealing, and it further increases by 900 degrees C annealing. The tendency of the Si-F bond peak absorption coefficient change is inverse to the change of FWHM, indicating that fluorine influences the Si-O bond nature. Other properties such as the **fluorine** atomic **concentration** , refractive index, etching rate, shrinkage, residual stress, and leakage current density are changed by the annealing. These property changes are due to changes in the chemical bonding structure. No crack is observed for the **SiOF films** formed on **aluminum wiring** patterns after 400 degrees C annealing.
Subfile: B

32/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5208855 INSPEC Abstract Number: A9608-8115H-012, B9604-0520F-110
Title: Characteristics of **SiOF** films formed using tetraethylorthosilicate and fluorotriethoxysilane at room temperature by chemical vapor deposition
Author(s): Homma, T.
Author Affiliation: ULSI Device Dev. Lab., NEC Corp., Sagamihara, Japan
Journal: Journal of the Electrochemical Society vol.143, no.2 p. 707-11
Publisher: Electrochem. Soc,
Publication Date: Feb. 1996 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
SICI: 0013-4651(199602)143:2L.707:CSFF;1-K
Material Identity Number: J010-96002
U.S. Copyright Clearance Center Code: 0013-4651/96/$7.00
Language: English
Abstract: The characteristics of **SiOF** films deposited using tetraethylorthosilicate (TEOS) and fluorotriethoxysilane [FTES: FSi(OC/sub 2/H/sub 5/)/sub 3/] at room temperature by chemical vapor deposition (RTCVD) have been studied. The RTCVD technique utilizes FTES, TEOS, and pure water as gas sources. The **SiOF** films are deposited by changing the FTES concentration in TEOS and FTES gas mixtures. The **SiOF** film deposition does not occur without the presence of FTES gas. The deposition rate increases with increasing the FTES concentration, then saturates at about 12 nm/min while the FTES concentration is 80%. The relationship between the film deposition rate and the FTES percentage in TEOS and FTES gas mixture is not linearly proportional. The deposited **SiOF** film properties such as refractive index, Si-O bond nature, residual OH content, etching rate (1:30 buffered hydrofluoric acid), and leakage current are almost independent of the FTES concentration in the range from 20 to 100%. Residual **fluorine concentrations** for the **SiOF** films deposited at the FTES concentrations of 20, 50, 80, and 100% are 1.91*10/sup 21/, 1.82*10/sup 21/, 1.51*10/sup 21/, and 1.51*10/sup 21/ atom/cm/sup 3/, respectively. The conformability of the **SiOF films** on **Al wiring** patterns is close to 100%. The formation mechanism of **SiOF** film is then described in a series of five chain reactions.
Subfile: A B

32/3,AB/3 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

04957316 Genuine Article#: UV530 Number of References: 14
Title: INSTABILITY OF SI-F BONDS IN FLUORINATED SILICON-OXIDE (**SIOF**) FILMS FORMED BY VARIOUS TECHNIQUES (Abstract Available)
Author(s): HOMMA T
Corporate Source: SHIBAURA INST TECHNOL,DEPT ELECTR,MINATO KU,3-9-14 SHIBAURA/TOKYO 108//JAPAN/; NEC CORP LTD,ULSI,DEVICE DEV LABS/SAGAMIHARA/KANAGAWA 229/JAPAN/
Journal: THIN SOLID FILMS, 1996, V278, N1-2 (MAY 15), P28-31
ISSN: 0040-6090
Language: ENGLISH Document Type: ARTICLE
Abstract: Instability of Si-F bonds in fluorinated silicon oxide (**SiOF**) **films** is studied. **Al wiring** corrosion and underlayer SiO2 etching problems are the major issues for the use of **SiOF** interlayer dielectric films. To clarify the mechanism, three kinds of **SiOF** films have been used for this study. They are: (i) a fluorinated silicon oxide (**SiOF**) film prepared by room-temperature chemical vapour deposition (RTCVD) using fluorotriethoxysilane and pure water as gas sources; (ii) a fluorinated spin-on-glass (SOG) film prepared by fluorotrialkoxysilane vapor treatment (FAST); and (iii) a room-temperature liquid phase deposition (LPD) **SiOF** film. The initial refractive indices fur the RTCVD-**SiOF**, FAST-SOG and LPD-**SiOF** films are 1.400, 1.398 and 1.433, respectively. After conducting a pressure cooker test (PCT) at 125 degrees C for 520 h, the refractive indices for the RTCVD-**SiOF**, FAST-SOG and LPD-**SiOF** films increase to 1.450, 1.440 and 1.436, respectively. The Si-O bond peak absorption coefficient for the LPD-**SiOF** film decreases at the early stage of PCT, but those for the RTCVD-**SiOF** and FAST-SOG films increase at the early stage of PCT. The initial Si-F bond peak absorption coefficient for the RTCVD-**SiOF** film is much higher than those for the LPD-**SiOF** and FAST-SOG films. It decreases drastically in the PCT time ranging from 0 to 140 h. The Si-F bond peak absorption coefficients for the FAST-SOG and LPD-**SiOF** films show a slow reduction, as compared with that for the RTCVD-**SiOF** film at the early stage of PCT. Although the OH peak absorption coefficients for the RTCVD-**SiOF** and FAST-SOG films increase at the early stage of PCT and level off at 50 h, that for the LPD-**SiOF** film increases at 306 h. After conducting 520 h PCT, **concentrations** of **fluorine** atoms for the RTCVD-**SiOF** and FAST-SOG films decrease by three orders and two orders of magnitudes, respectively. However, the LPD-**SiOF** film has a limited change in the **fluorine concentration**, as compared with those for the RTCVD-**SiOF** and FAST-SOG films. The thicknesses for all of the films remain almost unchanged after PCT for 520 h.

33/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012837001
WPI Acc No: 2000-008833/200001
XRAM Acc No: C00-001560
XRPX Acc No: N00-008062

Wiring layer for semiconductor device - has layer insulation film with **fluorine concentration** higher in wiring portion than on wiring

Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE)
Inventor: IMAI K; ODA N
Number of Countries: 004 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11289012	A	19991019	JP 9891538	A	19980403	200001	B
CN 1231504	A	19991013	CN 99103534	A	19990402	200008	
KR 99082907	A	19991125	KR 9911693	A	19990402	200055	
US 6274476	B1	20010814	US 99275532	A	19990324	200148	
US 20020011675	A1	20020131	US 99275532	A	19990324	200210	
			US 2001863737	A	20010523		
KR 320883	B	20020204	KR 9911693	A	19990402	200255	

Priority Applications (No Type Date): JP 9891538 A 19980403
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11289012	A		7	H01L-021/768	
CN 1231504	A			H01L-021/31	
KR 99082907	A			H01L-021/768	
US 6274476	B1			H01L-021/4763	
US 20020011675	A1			H01L-023/48	Div ex application US 99275532 Div ex patent US 6274476
KR 320883	B			H01L-021/768	Previous Publ. patent KR 99082907

Abstract (Basic): JP 11289012 A

NOVELTY - The **fluorine concentration** of **SiOF** layer insulation films (11,16) in the wiring portion are higher than **fluorine concentration** of **SiOF** layer insulation **films** (12,17) on **wiring**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of semiconductor device.

USE - For semiconductor device with multilayered interconnection structure using **SIOF** as insulating film.

ADVANTAGE - Reduces wiring capacity. Prevents debonding of an **interlayer film** on the **wiring**.

DESCRIPTION OF DRAWING - The figure shows the sectional view of semiconductor device. (11,12,16,17) **SiOF** layer insulation films.

Dwg.1/14

36/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06426976
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 2000-012539 [JP 2000012539 A]
PUBLISHED: January 14, 2000 (20000114)
INVENTOR(s): KOYANAGI KENICHI
APPLICANT(s): NEC CORP
APPL. NO.: 10-169778 [JP 98169778]
FILED: June 17, 1998 (19980617)

ABSTRACT

PROBLEM TO BE SOLVED: To enable avoidance of deterioration of an adhesion between an interlayer insulating film and a barrier metal or **wiring layer**, when a **wiring** groove is made in a silicon oxide film containing fluorine as the **interlayer** insulating **film** and the **wiring layer** is formed in the groove through a barrier metal of Ti, etc.

SOLUTION: The manufacturing method includes steps of forming an **SiOF** film 102 on a substrate 101, forming an **opening** for **wiring** formation in the **SiOF** film, removing fluorine contained in the **SiOF** film from a surface of the opening, subjecting the fluorine-removed surface of the opening to an oxygen plasma process, and providing wiring metals 104 and 105 to the opening.

36/3,AB/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05697533
METHOD OF FORMING INSULATING FILM

PUB. NO.: 09-312333 [JP 9312333 A]
PUBLISHED: December 02, 1997 (19971202)
INVENTOR(s): MUROYAMA MASAKAZU
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-126618 [JP 96126618]
FILED: May 22, 1996 (19960522)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method of forming an insulating film with low permittivity and high resistance to water permeability.

SOLUTION: In a method of forming an insulating film 14 to stop the **gap** between **wirings** on a substrate 11 provided with wirings 13, a base insulating film 14a consisting of silicon oxide is grown on the substrate 11 by a chemical growth method in an atmosphere where a plasma is created in high density. Next, an upper insulating film 14b consisting of **silicon oxide fluoride** is grown, in such a condition as to stop the **gap** between **wirings** 13, on the base insulating film 14a. Then, an insulating film 14 consisting of a lower insulating film 14a and an upper insulating film 14b is made.

43/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02376027 JICST ACCESSION NUMBER: 95A0470953 FILE SEGMENT: JICST-E
MUMIC approves effect of **layer insulation film** and flat **SiOF** film on hygroscopicity.
HOKO HIROMASA (1)
(1) Fujitsu Miekojo
Gekkan Semiconductor World(Semiconductor World), 1995, VOL.14,NO.5, PAGE.33-36, TBL.6
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The **first** DUMIC (**Dielectrics** & CMP For ULSI Multilevel Interconnection Conference in Santa Clara, February 21 - 22) was held. This is an international conference on **layer insulation film** of **multilayer wiring** and flattening of the film. During the conference, including the poster session, there were 51 presentations on gap film, CMP,SOG process and others. The most noticeable subject was **SiOF** film with improved absorbency.

43/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014234228
WPI Acc No: 2002-054926/200207
XRAM Acc No: C02-015605
XRPX Acc No: N02-040516
Manufacture of semiconductor integrated circuit device includes forming cap conductive **film** on **wiring** by selective or preferential growth
Patent Assignee: HITACHI LTD (HITA); IMAI T (IMAI-I); NOGUCHI J (NOGU-I); OHASHI N (OHAS-I); SAITO T (SAIT-I); TAMARU T (TAMA-I)
Inventor: IMAI T; NOGUCHI J; OHASHI N; SAITO T; TAMARU T
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010045651	A1	20011129	US 2001850162	A	20010508	200207	B
JP 2001319928	A	20011116	JP 2000135041	A	20000508	200208	
KR 2001105158	A	20011128	KR 200117834	A	20010404	200233	
TW 483105	A	20020411	TW 2001105990	A	20010314	200313	

Priority Applications (No Type Date): JP 2000135041 A 20000508
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010045651	A1		47	H01L-021/4763	
JP 2001319928	A		42	H01L-021/3205	
KR 2001105158	A			H01L-021/768	
TW 483105	A			H01L-021/768	

Abstract (Basic): US 20010045651 A1
Abstract (Basic):

NOVELTY - A semiconductor integrated circuit device is manufactured by forming a barrier layer (26a) and a conductive **film** (26b) inside a **wiring** groove (25) on a semiconductor substrate; removing the barrier layer and the conductive film from outside of the wiring groove to form a wiring (26); and forming a cap conductive **film** (26c) on the **wiring** by selective or preferential growth.

DETAILED DESCRIPTION - Manufacture of a semiconductor integrated circuit device comprises

(a) forming a wiring groove in a **first insulating film** formed on a semiconductor substrate;

(b) successively forming a barrier **layer** and a conductive **film** over the **first insulating film**, including the inside of the wiring groove, and removing the barrier layer and the conductive film from outside of the wiring groove to form a wiring;

(c) forming a cap conductive **film** on the **wiring** by selective or preferential growth; and

(d) forming a **second insulating film** over the cap conductive **film** and the **first insulating film**.

USE - For manufacturing a semiconductor integrated circuit device (claimed).

ADVANTAGE - The method provides a high-speed semiconductor integrated circuit device with elongated wiring life and suppressed electromigration or stress migration. When a contact hole formed on the wiring is etched at the bottom, direct sputtering of the underlying

wiring can be prevented. Thus, dielectric breakdown is improved, the reduction of a leakage current can be realized, the contact can be maintained, and contact failure can be reduced.

DESCRIPTION OF DRAWING(S) - The figures are sectional views showing the inventive method.

Wiring groove (25)
Barrier layer (26a)
Conductive film (26b)
Cap conductive film (26c)
pp; 47 DwgNo 6a, 6b/30

43/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014227945
WPI Acc No: 2002-048643/200206
XRAM Acc No: C02-013572
XRPX Acc No: N02-035971
Manufacture of semiconductor device involves etching organic low **dielectric** constant **film** using ammonia-containing gas
Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE); NAMBU H (NAMB-I)
Inventor: NAMBU H
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010034137	A1	20011025	US 2001836286	A	20010418	200206	B
JP 2001308175	A	20011102	JP 2000120337	A	20000421	200206	
KR 2001098774	A	20011108	KR 200121384	A	20010420	200227	
TW 486755	A	20020511	TW 2001109694	A	20010420	200323	

Priority Applications (No Type Date): JP 2000120337 A 20000421
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010034137	A1		16	H01L-021/302	
JP 2001308175	A		9	H01L-021/768	
KR 2001098774	A			H01L-021/311	
TW 486755	A			H01L-021/304	

Abstract (Basic): US 20010034137 A1
Abstract (Basic):
NOVELTY - Manufacture of a semiconductor device involves etching an organic low **dielectric** constant **film** using a silicon-containing **insulating film** as a mask. Etching is carried out using a gas comprising ammonia.
DETAILED DESCRIPTION - Manufacture of a semiconductor device comprises: forming an organic low **dielectric** constant **film** (2) on a substrate (1); forming a silicon-containing **insulating film** (3) on the organic low **dielectric** constant **film**; removing a part of the **insulating film** on the organic low **dielectric** constant **film**; removing a part of the silicon-containing **insulating film** to form a first opening (5); and etching the low **dielectric** constant **film** using the silicon-containing **insulating layer** with the **first** opening as a first mask. Etching is carried out using a gas comprising ammonia (NH3).
USE - None given.
ADVANTAGE - The method etches a organic low **dielectric** constant **film** with high precision without forming a bow-shaped cross-section of a via hole formed in the organic low **dielectric** constant **film** or causing shoulder drop of a silicon-containing **insulating film** employed as an etching mask for the organic low **dielectric** constant **film**.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a semiconductor device having a **multilayer wiring** structure.

Substrate (1)
Organic low **dielectric** constant **film** (2)
Silicon-containing **insulating film** (3)
Opening (5)
pp; 16 DwgNo 4E/5

43/3,AB/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06099150
MULTILAYERED WIRING STRUCTURE AND ITS MANUFACTURE

PUB. NO.: 11-040669 [JP 11040669 A]
PUBLISHED: February 12, 1999 (19990212)
INVENTOR(s): YAMADA YOSHIAKI
APPLICANT(s): NEC CORP
APPL. NO.: 09-194429 [JP 97194429]
FILED: July 18, 1997 (19970718)

ABSTRACT

PROBLEM TO BE SOLVED: To embed an **insulating film** without any clearance between micro- wiring by using a PE-CVD (plasma chemical vapor phase epitaxy) method.

SOLUTION: After a first wiring 3 has been formed, a **first interlayered insulating film** 4 is formed to be thin, that is, almost 200 nm by an HDP(high density plasma)-CVD method. At that time, high-frequency bias is impressed to a silicon substrate 1, and sputter etching is simultaneously operated with film formation so that a successive taper shape whose upper part is wide and whose bottom part is narrow can be formed between a wiring 3. Afterwards, a **second interlayered insulating film** 5 is formed by a PE-CVD method, and at that time, gas including F as components for chemically etching the **insulating film**, for example, C2F6 is added so that an **SiOF** film or the like can be formed. The etching is carried out at the same time with the film formation, so that difference in level coatability can be made satisfactorily, and the base is formed into the successively taper shapes, so that the film formation can be attained without clearances between the micro-wiring.

43/3,AB/5 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05758285
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 10-041385 [JP 10041385 A]
PUBLISHED: February 13, 1998 (19980213)
INVENTOR(s): MATSUMOTO AKIRA
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-190657 [JP 96190657]
FILED: July 19, 1996 (19960719)

ABSTRACT

PROBLEM TO BE SOLVED: To facilitate manufacturing of a buried wiring and effectively reduce the parasitic capacitance of the wiring, by forming an **insulation film** having a higher etching rate and lower specific dielectric const. than those of an **insulation film** beneath a **wiring** pattern on a region between the wiring patterns.

SOLUTION: The device has a **first insulation film** 11 on element regions on a semiconductor substrate 10 or **wiring layer** and **wiring** pattern 17' on this film 11. It also has a **second insulation film** 12 having a higher etching rate and lower specific dielectric const. than those of the first film 11 at least at a region formed between the patterns 17'. A first silicon oxide film 11 is deposited e.g. on the semiconductor substrate 10 having element regions, and **SiOF** film 12 is deposited thereon and used as an etching stopper to form wiring grooves 13. After forming contact holes 14, a second silicon oxide film 15, TiN film 16 and Al 17 are deposited to form the wiring 17'.

43/3,AB/6 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05739364
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 10-022464 [JP 10022464 A]
PUBLISHED: January 23, 1998 (19980123)
INVENTOR(s): ARITA KOJI
FUJII EIJI
UEMOTO YASUHIRO
NAGANO YOSHIHISA
MATSUDA AKIHIRO
APPLICANT(s): MATSUSHITA ELECTRON CORP [000584] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-173724 [JP 96173724]
FILED: July 03, 1996 (19960703)

ABSTRACT

PROBLEM TO BE SOLVED: To provide an excellent semiconductor device and manufacture thereof in which the electric property of a transistor is stabilized by recovery from interface damage while deterioration is not generated in characteristics of a capacitance element having a high **dielectric film** as a capacitance **insulating film**, by forming an **insulating film** on a **wiring** between **wiring layers** except for the portion on the capacitance element, then carrying out heat treatment, and then forming a protective film.

SOLUTION: A third **insulating film** 18 covering **first** wirings 17a, 17b except for the portion on a capacitance element 10, and a fourth **insulating film** 22 made of a silicon oxide film or a **silicon oxide fluoride** film covering the portion on the capacitance element 10 and the third **insulating film** 18, are formed. In the third **insulating film** 18 and the fourth **insulating film** 22, **second** contact holes 23a, 23b extending to the first wirings 17a, 17b are formed. Through these second contact holes, second wirings 24a, 24b made of a conductive material, such as, Al, are formed. In addition, a protective film 14 covering these second wirings is formed.

43/3,AB/7 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

05467999
WIRING BOARD AND MANUFACTURE THEREOF

PUB. NO.: 09-082799 [JP 9082799 A]
PUBLISHED: March 28, 1997 (19970328)
INVENTOR(s): FURUSAWA KENJI
KUSUKAWA KIKUO
HONMA YOSHIO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI CHEM CO LTD [000445] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-235000 [JP 95235000]
FILED: September 13, 1995 (19950913)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a wiring board having small electrostatic capacitance between adjacent wirings and a flat **insulating layer** surface **coating** the **wiring** at a low cost by a method wherein a **second insulating layer** consisting of an organic silicon compound is formed on the surface of a **first insulating layer** and the intervals between the adjacent wirings are filled with both the **first** and **second insulating layers**.

SOLUTION: In order to reduce electrostatic capacitance between adjacent lower **layer wiring** patterns 2, intervals between the adjacent lower **layer wiring** patterns 2 are filled by using a **first insulating layer** 4a consisting of a low dielectric coefficient **SiOF** and a **second insulating layer** 5 consisting of organic SOG of a low dielectric coefficient. In order to lower the cost, a film thickness of the **first insulating layer** 4a is made not exceeding 40%, preferably not exceeding 20% of the intervals between the adjacent lower **layer wiring** patterns 2. For instant, in the case of 5.mu.m of the wiring interval, the thickness of the **first insulating layer** 4a is made not exceeding 0.2.mu.m, preferably not exceeding 0.1.mu.m.

43/3,AB/8 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

05193062
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 08-148562 [JP 8148562 A]
PUBLISHED: June 07, 1996 (19960607)
INVENTOR(s): USAMI TAKASHI
YOSHIMARU MASAKI
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-285211 [JP 94285211]
FILED: November 18, 1994 (19941118)

ABSTRACT

PURPOSE: To realize both high performance and high reliability while using a fluorine added silicon oxide **film** as a **layer insulation film** by providing a film of low water absorption property which prevents hydrogen fluoride and fluorine from diffusing to at least either of an upper layer or a lower layer of the fluorine added silicon oxide film.

CONSTITUTION: A fluorine containing silicon oxide film (**SiOF** film) 17 is used as a **layer insulation film** of a semiconductor integrated circuit. In such a semiconductor device, a film 16 of low water absorption property which prevents hydrogen fluoride and fluorine from diffusing is provided to at least either of an upper **layer** or a lower **layer** of a **first insulation film** cosisting of the **SiOF** film 17 as a **second insulation film**. For example, a gate electrode 13, a **layer insulation film** 14 and a first metallic **wiring layer** 15 are provided on a semiconductor substrate 11 wherein an impurity diffusion layer 12 is formed. The **SiOF** film 17 is provide thereon with a silicon nitride film 16 of low water absorption property which prevents hydrogen fluoride and fluorine from diffusing through.

44/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5362062 INSPEC Abstract Number: A9619-6855-094
Title: Instability of Si-F bonds in fluorinated silicon oxide (**SiOF**) films formed by various techniques
Author(s): Homma, T.
Author Affiliation: ULSI Device Dev. Labs., NEC Corp., Kanagawa, Japan
Journal: Thin Solid Films vol.278, no.1-2 p.28-31
Publisher: Elsevier,
Publication Date: 15 May 1996 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
SICI: 0040-6090(19960515)278:1/2L.28:IBFS;1-K
Material Identity Number: T070-96014
U.S. Copyright Clearance Center Code: 0040-6090/96/$15.00
Language: English
Abstract: Instability of Si-F bonds in fluorinated silicon oxide (**SiOF**) **films** is studied. Al **wiring** corrosion and underlayer SiO/sub 2/ etching problems are the major issues for the use of **SiOF interlayer dielectric films**. To clarify the mechanism, three kinds of **SiOF** films have been used for this study. They are: (i) a fluorinated silicon oxide (**SiOF**) film prepared by room-temperature chemical vapour deposition (RTCVD) using fluorotriethoxysilane and pure water as gas sources; (ii) a fluorinated spin-on-glass (SOG) film prepared by fluorotrialkoxysilane vapor treatment (FAST); and (iii) a room-temperature liquid phase deposition (LPD) **SiOF** film. The initial refractive indices for the RTCVD-**SiOF**, FAST-SOG and LPD-**SiOF** films are 1.400, 1.398 and 1.433, respectively. After conducting a pressure cooker test (PCT) at 125 degrees C for 520 h, the refractive indices for the RTCVD-**SiOF**, FAST-SOG and LPD-**SiOF** films increase to 1.450, 1.440 and 1.436, respectively. The Si-O bond peak absorption coefficient for the LPD-**SiOF** film decreases at the early stage of PCT, but those for the RTCVD-**SiOF** and FAST-SOG films increase at the early stage of PCT. The initial Si-F bond peak absorption coefficient for the RTCVD-**SiOF** film is much higher than those for the LPD-**SiOF** and FAST-SOG films.
Subfile: A

44/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

4759288 INSPEC Abstract Number: B9410-2570D-035
Title: Reduction of wiring capacitance with new low **dielectric SiOF interlayer film** for high speed/low power sub-half micron CMOS
Author(s): Ida, J.; Yoshimaru, M.; Usami, T.; Ohtomo, A.; Shimokawa, K.; Kita, A.; Ino, M.
Author Affiliation: VLSI Res. & Dev. Center, Oki Electr. Ind. Co. Ltd., Tokyo, Japan
p.59-60
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA xv+168 pp.
ISBN: 0 7803 1921 4
U.S. Copyright Clearance Center Code: 0 7803 1921 4/94/$3.00
Conference Title: Proceedings of 1994 VLSI Technology Symposium
Conference Date: 7-9 June 1994 Conference Location: Honolulu, HI, USA
Language: English
Abstract: In sub-half micron CMOS, reduction of wiring capacitance is a key issue to improve the circuit performance because the ratio of wiring delay to total delay is increasing. In order to reduce the wiring capacitance, applying low dielectric materials to ULSI is most effective and developments of low dielectric materials have been reported recently. However, there have been no studies of applying those to sub-half micron CMOS. In this study, it is reported for the first time that the new low dielectric material **"SiOF "** which has been proposed previously has been applied to sub-half micron CMOS and the improvement of circuit performance has been confirmed. Moreover, it is clearly demonstrated that the **SiOF** film is inevitable to improve the circuit speed of 0.35 mu m CMOS with the scaling trend. Also, it is emphasized that the reduction of **wiring** capacitance with **SiOF film** is important from the viewpoint of power reduction in sub-half micron CMOS.
Subfile: B

44/3,AB/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015228261
WPI Acc No: 2003-289174/200328
XRAM Acc No: C03-075064
XRPX Acc No: N03-229998
Semiconductor device e.g. memory has **wiring interlayer insulating film** having low permittivity and covered by hard mask
Patent Assignee: NEC CORP (NIDE); NAMBU H (NAMB-I)
Inventor: NAMBU H
Number of Countries: 032 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030020176	A1	20030130	US 2002205196	A	20020725	200328 B
JP 2003045964	A	20030214	JP 2001230600	A	20010730	200328
EP 1282165	A2	20030205	EP 2002291912	A	20020729	200328

Priority Applications (No Type Date): JP 2001230600 A 20010730
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030020176	A1		39	H01L-023/48	
JP 2003045964	A		19	H01L-021/768	
EP 1282165	A2	E		H01L-021/768	

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): US 20030020176 A1
Abstract (Basic):
NOVELTY - An **interlayer insulating film** (5) that is formed over an underlayer wiring (2), has low permittivity and is covered by a hard mask (7). A through-plug (13) and an upper **layer wiring** (14) are simultaneously formed in a through-hole (11) and a wiring trench (12) that are formed in the **insulating film**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for semiconductor device manufacturing method.
USE - Semiconductor device e.g. memory and microprocessor.
ADVANTAGE - Reduces the inter-wiring capacitance arising from the **interlayer insulating films**, thereby suppressing signal delay and increasing operation speed.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the semiconductor device.
underlayer wiring (2)
interlayer insulating film (5)
hard mask (7)
through-hole (11)
wiring trench (12)
through-plug (13)
upper **layer wiring** (14)
pp; 39 DwgNo 3/24

44/3,AB/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013677399
WPI Acc No: 2001-161612/200117
XRAM Acc No: C01-048396
XRPX Acc No: N01-117897
Wiring layer formation method for semiconductor device manufacture - involves forming **SiOF film** on **insulating film** followed by vent formation and deposition of metal for wiring
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000012539	A	20000114	JP 98169778	A	19980617	200117	B

Priority Applications (No Type Date): JP 98169778 A 19980617
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000012539	A		10	H01L-021/3205	

Abstract (Basic): JP 2000012539 A

NOVELTY - The **SiOF** film (102) is formed on substrate (101) followed by vent formation for wiring. The fluorine on vent area is removed from **SiOF** film followed by oxygen plasma treatment on surface of vent. Titanium (104) and copper (105) are deposited on the vent.

USE - For semiconductor device such as ULSI manufacture.

ADVANTAGE - The deposition of copper and titanium on vent area, reduces degradation of background film and prevents damages to **wiring layer.**

DESCRIPTION OF DRAWING(S) - The figure shows sectional view of **wiring** formation on **SiOF film** provided on semiconductor substrate. (101) Substrate; (102) **SiOF** film; (104) Titanium; (105) Copper.

Dwg.1/16

44/3,AB/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013331352
WPI Acc No: 2000-503291/200045
XRAM Acc No: C01-001961
XRPX Acc No: N01-005458
Insulation film formation in semiconductor device manufacture, involves forming lower HSQ film having material with low **dielectric** constant by spin **coating**, on semiconductor substrate
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM S J; PARK H S; SHIN H J; KIM S; PARK H; SHIN H
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 99057679	A	19990715	KR 9777745	A	19971230	200045	B
JP 11204645	A	19990730	JP 98157853	A	19980605	200102	
US 6277764	B1	20010821	US 98224560	A	19981230	200150	
KR 292403	B	20010712	KR 9777745	A	19971230	200226	

Priority Applications (No Type Date): KR 9777745 A 19971230
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 99057679	A			H01L-021/31	
JP 11204645	A		4	H01L-021/768	
US 6277764	B1			H01L-021/31	
KR 292403	B			H01L-021/31	Previous Publ. patent KR 99057679

Abstract (Basic): JP 11204645 A
Abstract (Basic):
NOVELTY - The lower HSQ film having material with low dielectric constant is formed by spin coating, on surface of semiconductor substrate (10) formed with metallic wiring (12). The upper **SiOF** film (32) containing material with low dielectric constant is formed on HSQ film by high density plasma chemical vapor deposition (PCVD) technique. The **SiOF** film is planarized by chemo mechanical polishing.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **insulation film**.
USE - For forming double **layered** insulation **film** on metallic **wiring** in manufacture of semiconductor integrated circuit device.
ADVANTAGE - Since **insulation films** contain material with low dielectric constant, parasitic capacitance is reduced. Simplifies planarizing processes involved by accurately performing spin coating and PCVD of respective **insulation film**.
DESCRIPTION OF DRAWING(S) - The figure depicts sectional view of substrate.
Semiconductor substrate (10)
Metallic wiring (12)
Lower HSQ film (22)
Upper **SiOF** film (32)
pp; 4 DwgNo 4/4

44/3,AB/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013113930
WPI Acc No: 2000-285801/200025
XRAM Acc No: C00-086471
XRPX Acc No: N00-215242
Wiring layer of semiconductor integrated circuit, has **insulating film** between **wiring layers** which contains fluorine formed on titanium silicide
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000077415	A	20000314	JP 98248796	A	19980905	200025	B

Priority Applications (No Type Date): JP 98248796 A 19980902
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000077415	A		6	H01L-021/3205	

Abstract (Basic): JP 2000077415 A
Abstract (Basic):
NOVELTY - Titanium silicide film (108) is formed on a portion of diffused layer (106). The titanium silicide surface is covered by titanium nitride **film** (109). **SiOF insulating film** between **wiring layers** which contain fluorine, is formed on titanium silicide.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **wiring layer** formation method.
USE - For gate electrode of transistor, in semiconductor integrated circuit.
ADVANTAGE - Since **SiOF insulating film** is formed on titanium silicide, reaction of fluorine is prevented. Hence combination of titanium silicide diffused **layer**, **wiring** and silicon oxide **film** are made possible. Therefore high speed semiconductor device with secured favorable **layer insulation** capability can be obtained.
DESCRIPTION OF DRAWING(S) - The figure shows sectional view of manufacturing process of semiconductor device.
Diffused layer (106)
Titanium silicide film (108)
Titanium nitride film (109)
pp; 6 DwgNo 1/96

44/3,AB/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013037563
WPI Acc No: 2000-209415/200019
XRAM Acc No: C00-064834
XRPX Acc No: N00-156266
Multilayer interconnection structure of semiconductor device - has **SiOF film** formed between metal **wiring** and silicone nitride **film**, above which another SiO - 2 film is formed, with silicone nitride film having water diffusion suppression properties
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11111845	A	19990423	JP 97271134	A	19971003	200019	B

Priority Applications (No Type Date): JP 97271134 A 19971003
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11111845	A		8	H01L-021/768	

Abstract (Basic): JP 11111845 A

NOVELTY - A fluorine added silicon oxide **film** (31) separates the **wiring layer** (20) and the silicone nitride film (32), above which another SiO2 film (33) is formed, with relative dielectric constant higher than **SiOF** film (31), but lower than film (32). The silicone nitride film (32) has water or hydroxide ion diffusion suppression properties. DETAILED DESCRIPTION - An upper **wiring layer** (50) is formed on the upper **insulating film** (33). Plug material (41) is embedded in the hole, which is linked to wiring (20) and formed through the layers (31-33). An INDEPENDENT CLAIM is also included for semiconductor device manufacturing method.

USE - For semiconductor device.

ADVANTAGE - Spreading of impurities and penetration of water or hydroxide ion are prevented, thus improving reliability of semiconductor device. DESCRIPTION OF DRAWING(S) - The figure shows sectional view of **multilayer insulation film** interconnection structure. (20,50) **Wiring layers**; (31) **SiOF film**; (32) Silicone nitride film; (33) SiO2 film; (41) Plug material.

Dwg.1/8

44/3,AB/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012909460
WPI Acc No: 2000-081296/200007
XRAM Acc No: C00-023090
Formation of **insulating film** - for use in **multi layered wiring**
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11330062	A	19991130	JP 98128837	A	19980512	200007	B

Priority Applications (No Type Date): JP 98128837 A 19980512
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11330062	A		4	H01L-021/31	

Abstract (Basic): JP 11330062 A

NOVELTY - The formation of an **insulating film** comprises a process for forming an **insulating film** by applying the plazma chemical vapor accumulation process with the fluorine gas and an organic silicon compound. DETAILED DESCRIPTION - The formation of an **insulating film** comprises a process for forming an **insulating film** by applying the plazma chemical vapor accumulation process with the fluorine gas and an organic silicon compound represented by a general formula R1mSi(OR2)n; R1 = 1-4C hydrocarbon or aromatic hydrocarbon; R2 = 1-4C hydrocarbon.

USE - Effectively used for the **insulating film** of the **multilayered wiring** in an integrated circuit device.

ADVANTAGE - The CF bond can be effectively formed. The coating film is a fluorocarbon silicon oxide film, so that the increase of the dielectric constant caused by the humidity absorption which is found in a conventional **SiOF** film, can be prevented.

Dwg.0/0

44/3,AB/9 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012310635
WPI Acc No: 1999-116741/199910
XRAM Acc No: C99-034263
XRPX Acc No: N99-086329
Semiconductor device - has second **SiOF film** which has **dielectric** constant equal to or lower than that of first **SiOF** film, is formed on first **SiOF** film
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10340897	A	19981222	JP 97149154	A	19970606	199910	B

Priority Applications (No Type Date): JP 97149154 A 19970606
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10340897	A		6	H01L-021/316	

Abstract (Basic): JP 10340897 A
NOVELTY - The metal wiring (22) is formed on the main- surface side of a semiconductor substrate (21). A first **SiOF** film (13) is provided covering the metal **wiring**. A second **SiOF film** (14) which has **dielectric** constant equal to or lower than that of the first **SiOF** film, is formed on the **SiOF** film (13). DETAILED DESCRIPTION - An INDEPENDENT CLAIM is provided for manufacturing method of semiconductor device.
USE - None given.
ADVANTAGE - Prevents etching damage of metal **wiring**, during **film** formation. Enables formation of low **dielectric** constant **insulating film**. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of semiconductor device. (13) First **SiOF** film; (14) Second **SiOF** film; (21) Semiconductor substrate; (22) Metal wiring.
Dwg.1/4

44/3,AB/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012285738
WPI Acc No: 1999-091844/199908
XRAM Acc No: C99-027376
XRPX Acc No: N99-067789
Multilayered interconnection **wiring** structure manufacture for semiconductor device - involves forming **insulating** cap **film** containing hygroscopic low material, on polished **insulating film**
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10326829	A	19981208	JP 97134183	A	19970523	199908	B

Priority Applications (No Type Date): JP 97134183 A 19970523
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10326829	A		14	H01L-021/768	

Abstract (Basic): JP 10326829 A

The method involves covering a wiring formed on silicon substrate by a **SiOF film** (64) having **dielectric** constant of 3.5. An **insulating film** is formed on the **SiOF** film.

Then, the **insulating film** and **SiOF film** are polished and exposed. An **insulating** cap **film** (66) containing hygroscopic material, is formed on the polished **insulating film**.

ADVANTAGE - Prevents debonding of metal film from layer **insulation film** of low **dielectric** constant. Suppresses hygroscopic property of **SiOF** film for moisture proofs. Suppresses increase in **dielectric** constant of **SiOF film**.

Dwg.3/12

44/3,AB/11 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011768650
WPI Acc No: 1998-185560/199817
XRAM Acc No: C98-059069
XRPX Acc No: N98-147403
Wiring layer formation method for semiconductor device manufacture - involves forming wiring groove on low **dielectric** constant **film** which is deposited on first silicon oxide film
Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE)
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10041385	A	19980213	JP 96190657	A	19960719	199817	B
KR 98012612	A	19980430	KR 9734240	A	19970722	199917	
KR 258044	B1	20000601	KR 9734240	A	19970719	200130	

Priority Applications (No Type Date): JP 96190657 A 19960719
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10041385	A		7	H01L-021/768	
KR 98012612	A			H01L-029/76	
KR 258044	B1			H01L-021/768	

Abstract (Basic): JP 10041385 A

The method involves forming a first silicon oxide film (11) on the element area or **wiring layer** of a substrate (10). A low **dielectric** constant **film** such as a **SiOF** film (12) is deposited on the first silicon oxide film.

The **SiOF** film has a higher etching rate than the silicon oxide **film**. A **wiring** groove (13) is formed on the low **dielectric** constant **film** by anisotropic dry etching. A wiring metal is deposited on the whole surface containing the groove. Metals portions other than groove are removed by chemical mechanical polishing.

ADVANTAGE - Simplifies formation of groove wiring. Reduces wiring parasitic capacitance. Facilitates formation of implanting wiring.

Dwg.2/7

44/3,AB/12 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011400614
WPI Acc No: 1997-378521/199735
XRAM Acc No: C97-121701
XRPX Acc No: N97-314705
Semiconductor device mfr, e.g. for LSI - involves forming **insulating film** containing **silicon oxyfluoride** over processed substrate, by CVD process using thiocarbonyl fluoride, silane and oxidising gas mixture
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9162184	A	19970620	JP 95319048	A	19951207	199735	B

Priority Applications (No Type Date): JP 95319048 A 19951207
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9162184	A		6		

Abstract (Basic): JP 9162184 A

The method involves forming an **interlayer insulating film** (4) containing **SiOF** over a processed substrate (11) by CVD process. The process is carried out using a mixture of thiocarbonyl fluorides, silanes and oxidising gas.

An ultrasonic wave is applied to the processed substrate. The inner SiO2 layer receives equally the fluorine gas generated by decomposition of thiocarbonyl fluoride. The carbonyl residue formed is oxidised and removed out of the CVD chamber.

ADVANTAGE - The method avoids contamination, as carbonyl residue is removed; enables reliable semiconductor mfr, without any signal delay by **wiring layer**; and improves integration density of memory.

Dwg.1/2

44/3,AB/13 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010470803
WPI Acc No: 1995-372157/199548
XRAM Acc No: C95-161465
XRPX Acc No: N95-274283
Semiconductor device prepn. with stable permittivity - by laminating silicon oxide film contg. fluorine on substrate by PCVD using high and low frequency alternate electric field
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7254592	A	19951003	JP 9445920	A	19940316	199548	B

Priority Applications (No Type Date): JP 9445920 A 19940316
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7254592	A		8	H01L-021/31	

Abstract (Basic): JP 7254592 A
A silicon oxide film contg. F is laminated on a substrate by plasma CVD under excitation of reaction gas using high frequency and low frequency electric field simultaneously.
USE - The method is suitable for forming **insulating film** of **multilayer wiring.**
ADVANTAGE - A **SiOF** film is produced with stable permittivity at normal air atmos.
Dwg.2/7

44/3,AB/14 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07140776

METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

PUB. NO.: 2002-009148 [JP 2002009148 A]
PUBLISHED: January 11, 2002 (20020111)
INVENTOR(s): SHIMIZU AKIRA
OZAKI NORITOSHI
APPLICANT(s): ASM JAPAN KK
APPL. NO.: 2000-190620 [JP 2000190620]
FILED: June 26, 2000 (20000626)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method for manufacturing a semiconductor device where an **interlayer insulating film** having a hollow structure and a relative permittivity as near as 1 is formed by employing an oxide film having a high selectivity and carrying out a selective etching process.

SOLUTION: The method related to the present invention, i.e., the method for manufacturing the semiconductor device forming the **interlayer insulating film** of a **multilayer wiring** with the hollow structure, comprises (a) a step for forming a **SiOF** film **layer** 1 on a **wiring** 2, (b) a step for forming a cap film layer 3 on the **SiOF** film layer 1, (c) a step for penetrating the cap film layer 3 and the **SiOF** film layer 1 and forming a contact hole 4, (d) a step for forming the contact plug 5 so as to fill the contact hole 4 and search the wiring 2, (e) a step for forming an opening part 6 having a prescribed size at the cap film layer 3, (f) a step for aligning on the contact plug 5 and forming a wiring 7, (g) a step for repeating the above steps (a) to (f) only prescribed number of times, (h) a step for selectively etching all the **SiOF** layers of each stage of the multilayer structure, and (i) a step for sealing 10 the opening part at the cap film layer of the highest stage. Only HF is used as an etching gas.

44/3,AB/15 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06808359
MANUFACTURE OF SEMICONDUCTOR DEVICE AND METHOD FOR FORMATION OF **INSULATING FILM**

PUB. NO.: 2001-035844 [JP 2001035844 A]
PUBLISHED: February 09, 2001 (20010209)
INVENTOR(s): ENOMOTO YASUYUKI
APPLICANT(s): SONY CORP
APPL. NO.: 11-204635 [JP 99204635]
FILED: July 19, 1999 (19990719)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent the delamination of an **insulating film**.

SOLUTION: **Wiring layers** 2 are formed on a semiconductor substrate 1 and thereafter, an **SiOF** film 3 is formed on the whole surface of the substrate 1 by an HDP(High Density Plasma)-CVD method. The formation of this film 3 is performed under the condition where the amount of hydrogen, which is taken in the film 3, is suppressed. Specifically, the film 3 is formed using raw gas, which contains fluorine and oxygen and does not contain hydrogen. Or the film 3 is formed at a temperature higher than a temperature to reach the desorption peak of hydrogen in the heat-up and desorption characteristics of the film 3. After that, an SiO2 film 4 is formed using TEOS gas and a flattening of the surface of the film 4 is performed. Before an adhesive layer 6 is formed, a heat treatment is performed and the hydrogen is made to release from the film 3. After a film having an action to occlude hydrogen in a Ti film or the like is deposited as the layer 6, a W film 7 is formed by a blanket WCVD method.

44/3,AB/16 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06771813
MANUFACTURE FOR SEMICONDUCTOR DEVICE AND PLASMA CVD UNIT

PUB. NO.: 2000-357687 [JP 2000357687 A]
PUBLISHED: December 26, 2000 (20001226)
INVENTOR(s): MIYAJIMA HIDESHI
NAKADA RENPEI
KAWAI MOTONOBU
YAMADA NOBUHIDE
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 11-168619 [JP 99168619]
FILED: June 15, 1999 (19990615)

ABSTRACT

PROBLEM TO BE SOLVED: To form a lower permittivity **insulation film** without lowering reliability due to a degeneration layer by a method wherein temperatures of a semiconductor substrate are increased up to deposition temperatures of an **insulation film**.

SOLUTION: Not by a heating method by an oxygen ion impact, but by a heating method using a resistant heating heater, substrate temperatures are increased up to temperatures required for forming an **SiOF** film 4. Therefore, a CH3-SiO2 film is not oxidized. SiO4 and O2 as material gases are introduced into a reactive container at 20 SCCM and 40 SCCM, respectively, and the pressure is held at 5.0 mTorr, and induction power is set to be 2000 W, and the **SiOF** film 4 is formed on the entire surface by a high dense plasma CVD method. An Al **wiring** of a second **layer** and on is formed on the **SiOF** film 4. A degeneration layer which is a cause of generating HF is not formed, and therefore it is possible to form a lower permittivity **interlayer insulation film** by use of the high dense plasma CVD method without lowering reliability.

44/3,AB/17 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

06700431
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 2000-286262 [JP 2000286262 A]
PUBLISHED: October 13, 2000 (20001013)
INVENTOR(s): MATSUURA MASAZUMI
GOTO KINYA
APPLICANT(s): MITSUBISHI ELECTRIC CORP
APPL. NO.: 11-087521 [JP 9987521]
FILED: March 30, 1999 (19990330)

ABSTRACT

PROBLEM TO BE SOLVED: To provide the manufacture of a semiconductor device, which materializes one of such structures in which an F diffusion preventing film is not etched at formation of the metallic **wiring** of an upper **layer** and that an **SiOF** film is not polished directly by CMP method, in a semiconductor device equipped with an F diffusion preventing film for preventing the F atoms in the **SiOF** film from diffusing into the metallic **wiring** of an upper **layer**.

SOLUTION: In this manufacture, a first **layer** metallic **wiring** 2, an **SiOF film** 3, and an F diffusion preventing film 6 are formed on the surface of the base layer 1 including a substrate, an element made on the substrate, and an **insulating layer** formed to cover the substrate and the element. For this F diffusion preventing film 6, it is sufficient to adopt a silicon nitride film or a silicon oxide film which includes Si-H bonding. Then, a spacer film 4 is made on the surface of the F diffusion preventing film 6, and the surface is flattened. Then, the second **layer** metallic **wiring** 5 is formed on the surface of the spacer film 4.

44/3,AB/18 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

06412806
ELECTRONIC DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-354464 [JP 11354464 A]
PUBLISHED: December 24, 1999 (19991224)
INVENTOR(s): MUROYAMA MASAKAZU
APPLICANT(s): SONY CORP
APPL. NO.: 10-157899 [JP 98157899]
FILED: June 05, 1998 (19980605)

ABSTRACT

PROBLEM TO BE SOLVED: To improve contact between a barrier metal layer and a metal layer which are formed in contact with **SiOF**, by laminating in sequence the barrier metal layer containing a specified metal and a metal layer on a silicon oxide layer containing fluorine.

SOLUTION: An **interlayer insulating film** 2 and a **wiring layer** 3 are formed on a semiconductor substrate 1, and hence the **wiring layer** 3 forms a step. Then, a silicon oxide layer 4 containing fluorine is formed thereon and the surface of the layer 4 is planarized. In the silicon oxide layer 4 containing fluorine, a connection hole 6 is made to the **wiring layer** 3 and is filled with a contact plug made of a barrier metal layer 7 and a metal layer 8. The barrier metal 7 contains at least one element selected from the group consisting of Ta, Zr, TaN, and ZrN. This strengthens a metal-oxygen atomic bond and a metal-fluorine atomic bond at the interface between the silicon oxide layer 4 containing fluorine and the barrier metal layer 7.

44/3,AB/19 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

06084938
FORMATION OF **INSULATING FILM** AND SEMICONDUCTOR DEVICE

PUB. NO.: 11-026452 [JP 11026452 A]
PUBLISHED: January 29, 1999 (19990129)
INVENTOR(s): KOBAYASHI KINYA
FUKUDA TAKUYA
KATOU KIYOTAKA
APPLICANT(s): HITACHI LTD
APPL. NO.: 09-183475 [JP 97183475]
FILED: July 09, 1997 (19970709)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce the forming cost of an **insulating film** as much as possible, by combining a film forming a process using expensive SiH2F2 gas with another film forming process using inexpensive SiF4(+SiH4) gas.

SOLUTION: In a process 1, a plasma and, in its turn, various kinds of radicals are generated by ionizing SiH2F2 gas, O2 gas, and Ar gas by using a magnetic field generated from an electromagnet and microwaves, and parts of the insides of wiring grooves formed on the surface of a semiconductor wafer are filled up with an **SiOF** film. In a process 2, a plasma and, in its turn, various kinds of radicals are generated by introducing SiF4 gas and SiH4 gas to a film forming vessel, and parts of the insides of the wiring grooves formed on the surface of the semiconductor wafer are filled up with another **SiOF** film 23. When a film which is formed by a film forming method in which the processes 1 and 2 are combined together and has a small dielectric constant is used as an **interlayer insulating film**, the **wiring** delay or manufacturing cost of a semiconductor element resulting from an increased degree of integration can be suppressed as much as possible. Therefore, the manufacturing cost of highly integrated MPUs and DRAMs of the next generation can be reduced.

44/3,AB/20 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

05720987
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 10-004087 [JP 10004087 A]
PUBLISHED: January 06, 1998 (19980106)
INVENTOR(s): MUROYAMA MASAKAZU
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-154658 [JP 96154658]
FILED: June 14, 1996 (19960614)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor device having an **insulation film** having a low **dielectric** const. and superior embedding characteristic.

SOLUTION: A SiO(sub 2) **film** 2 and Al **wiring** pattern 3 are formed on a Si substrate 1, and this pattern 3 is covered with an **interlayer insulation film** 4 containing particles of a low dielectric const. inorganic compound in a resin. This compound is preferably one of **SiOF**, SiOBN, SiBN and BN. Adding of such particles of the compound reduces the resin's thermal expansion coefficient and raises its glass transition temperature

44/3,AB/21 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

05645570
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 09-260370 [JP 9260370 A]
PUBLISHED: October 03, 1997 (19971003)
INVENTOR(s): SATO JUNICHI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-069743 [JP 9669743]
FILED: March 26, 1996 (19960326)

ABSTRACT

PROBLEM TO BE SOLVED: To enable forming a silicon oxide-based **insulating film** containing fluorine wherein **dielectric** constant is sufficiently reduced and contamination and deterioration of hot carrier resistance which are to be caused by addition gas are eliminated, by using material gas whose main components are tetraisocyanate silane and thiocarbonyl fluoride.

SOLUTION: A silicon oxide-based **insulating film** 4 containing fluorine is formed on a substrate 11 to be treated by using a CVD method using material gas whose main components are tetraisocyanate silane and thiocarbonyl fluoride. One or more kinds out of CSF(sub 2) and CSF(sub 4) are suitable for the thiocarbonyl fluoride. For example, a **wiring layer** 3 composed of Al-base metal is formed on a **layer insulating film** 2 on a semiconductor substrate 1 of Si or the like, and turned into the substrate 11 to be treated. The **layer insulating film** 4 which is composed of **SiOF** and whose dielectric constant is 3.3 is formed on the substrate 11 by using a plasma CVD method wherein Si(NCO)(sub 4) of 50sccm and CSF(sub 2) of 30sccm are used as material gas.

44/3,AB/22 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

05645567
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 09-260367 [JP 9260367 A]
PUBLISHED: October 03, 1997 (19971003)
INVENTOR(s): SATO JUNICHI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-062250 [JP 9662250]
FILED: March 19, 1996 (19960319)

ABSTRACT

PROBLEM TO BE SOLVED: To enable forming an oxide silicon-based **insulating film** containing fluorine wherein **dielectric** constant is sufficiently reduced and contamination due to additional gas is eliminated, by using a CVD method using material gas whose main components are silane-based gas, oxidizing gas and chalcogen fluoride compound.

SOLUTION: An oxide silicon-based **insulating film** 4 containing fluorine is formed on a substrate 11 to be treated, by using a CVD method using material gas whose main components are silane-based gas, oxidizing gas and chalcogen fluoride compound. One or more kinds out of OF(sub 2), S(sub 2)F(sub 2), SF(sub 2), SF(sub 4), S(sub 2)F(sub 10), SeF(sub 4) and TeF(sub 4) are suitable for the chalcogen fluoride compound. For example, a **wiring layer** 3 composed of Al-based metal is formed on a **layer insulating film** 2 on a semiconductor substrate 1 of Si or the like, and it is made the substrate 11 to be treated. On the substrate 11, the **layer insulating film** 4 composed of **SiOF** is formed by using a plasma CVD method wherein SiH(sub 4) of 50sccm, O(sub 2) of 50sccm and S(sub 2)F(sub 2) of 30sccm are used as material gas.

44/3,AB/23 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

05617508
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 09-232308 [JP 9232308 A]
PUBLISHED: September 05, 1997 (19970905)
INVENTOR(s): SATO JUNICHI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-035226 [JP 9635226]
FILED: February 22, 1996 (19960222)

ABSTRACT

PROBLEM TO BE SOLVED: To form a silicon oxide based **insulating film** with a practical deposition rate which film is free from contamination and contains fluorine, by using a CVD method material gas whose main component is compound composed of silane based gas, oxidizing gas, rare gas atoms and fluorine atoms.

SOLUTION: A substrate 11 to be treated is constituted by forming a **wiring layer** 3 composed of Al based metal constituted of line and space of specified width, on an **interlayer insulating film** 2 on a semiconductor substrate 1 of Si or the like. The substrate 11 is mounted on the stage of a CVD equipment. A silicon oxide based **insulating film**(**SIOF**) containing fluorine is formed on the substrate 11 to be treated, by a CVD method using material gas whose main component is compound composed of silane based gas, oxydizing gas, rare gas atoms and fluorine atoms. Thereby an **interlayer insulating film** 4 is formed with a practical deposition rate which film is excellent in step coverage and composed of **SiOF** free from contamination of carbon and sulfur.